

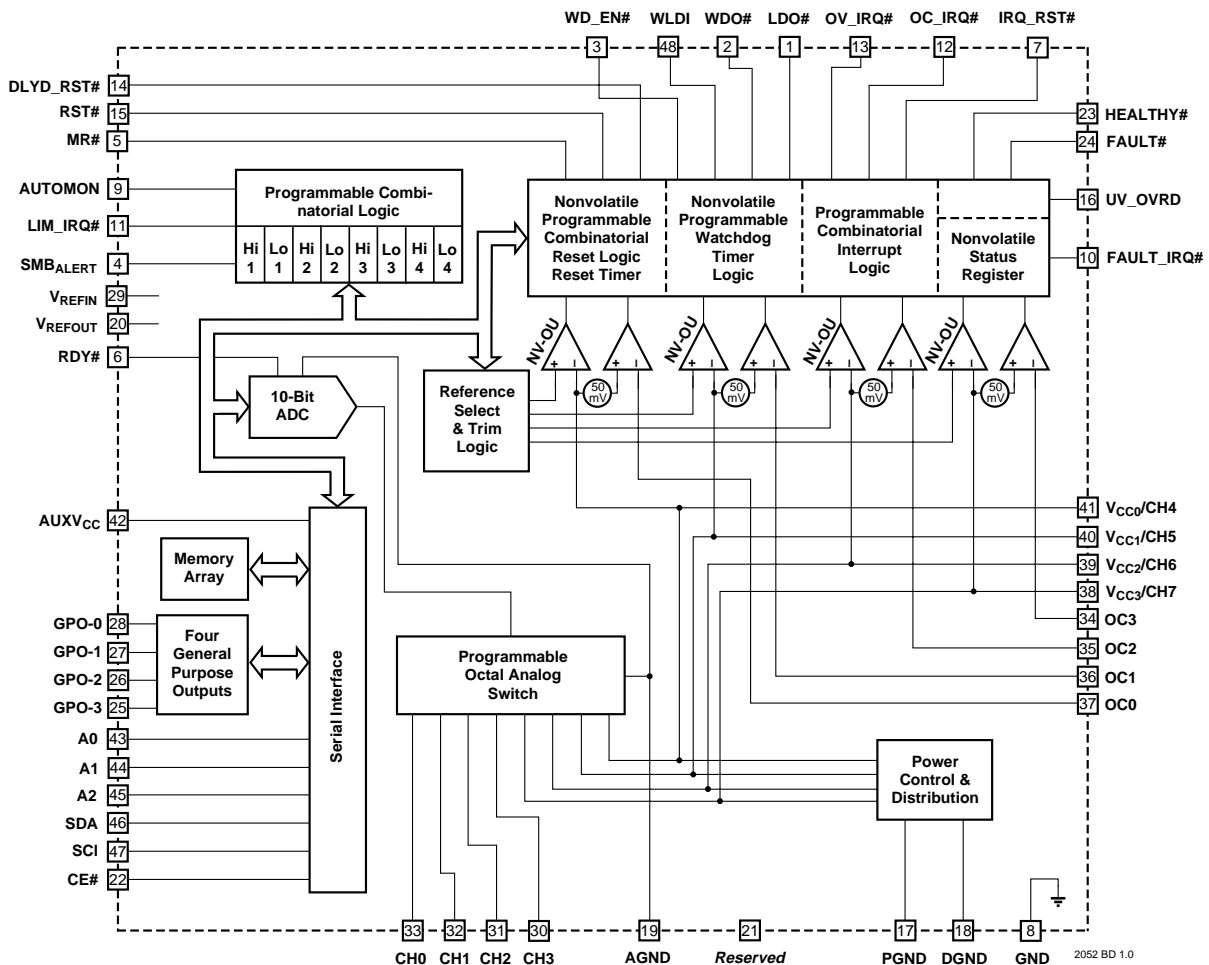


8-Channel Auto-Monitor™ ADC
In System Programmable Analog (ISPA™) Device

FEATURES

- Programmable 8 Channel 10-bit A to D converter
 - ◆ Programmable Sequencing of Analog Switches in Auto-Monitor Mode
 - ◆ Resolution 10 bits
 - ◆ DNL ± 1 LSB
 - ◆ Top 4 Channels Programmable, Nonvolatile Upper/Lower IRQ Limits
 - ◆ Bottom 4 Channels Tied to Matching Programmable, Nonvolatile Comparators
 - ◆ 4 Companion Over-current Comparators
- Programmable LED Driver Outputs
- Programmable, Nonvolatile Combinatorial Reset Logic
- Nonvolatile Status Capture Register
- Two Programmable, Nonvolatile Watchdog Timers
- 1K-bit Nonvolatile Memory
- Industry Standard 2-Wire Interface
 - ◆ Nonvolatile Configuration Registers
 - ◆ ADC Conversion Results
 - ◆ Memory Array
 - ◆ Mechanism for System Level Presence Detect

FUNCTIONAL BLOCK DIAGRAM



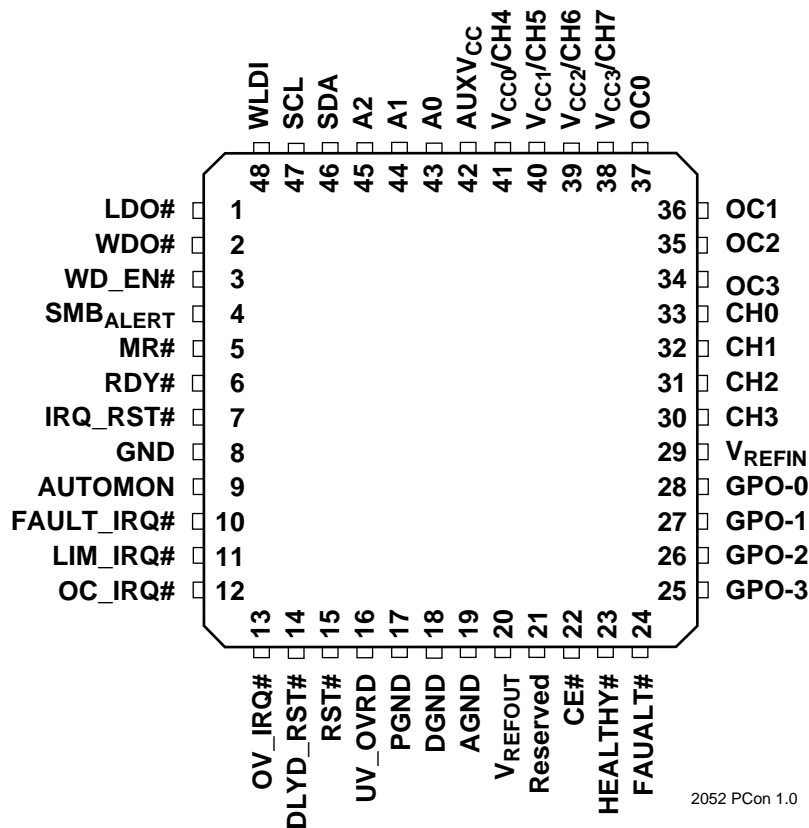


DESCRIPTION

The SMD1108 is a versatile, programmable 8-channel, 10-bit Data Acquisition System that is designed to operate autonomously, relieving the system host and logic board of the environmental monitoring tasks.

PIN CONFIGURATION

48-Pin TQFP



2052 PCon 1.0



ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	-55°C to 125°C	Group 2: RDY	-2V to 7V
Storage Temperature	-65°C to 150°C	Group 3: IRQ_RST#, WD_EN#, MR#, WLDI, SCL, CE#, A0, A1, A2, and AUTOMON	-2V to 7V
Lead Solder Temperature (10s)	300 °C	Analog Inputs: V _{CC0} /CH4, V _{CC1} /CH5, V _{CC2} /CH6, V _{CC3} /CH7, CH0, CH1, CH2, CH3, OC1, OC2, OC3, AUXV _{CC} , and V _{REFIN}	-2V to 7V
Output Short Circuit Current	① 100mA		
Terminal Voltage with Respect to GND (AGND, DGND & PGND tied):			
Group 1: LDO#, WDO#, SMB _{ALERT} #, HEALTHY#, FAULT_IRQ#, LIM_IRQ#, OC_IRQ#, RST#, OV_IRQ#, DLYD_RST#, FAULT#, GPO-0, GPO-1, GPO-2, and GPO-3	-2V to 7V		

① Output shorted for no more than one second, no more than one output shorted at a time.

DC OPERATING CHARACTERISTICS

(Over Recommended Operating Conditions; Voltages are relative to GND)

Symbol	Parameter	Conditions (Note 1)	Min.	Typ.	Max.	Units
I _{CC}	Supply Current	All outputs open				mA
I _{SB}	Standby Current	All outputs open, ADC idle, no memory in process				mA
I _{LI}	Input leakage current	V _{IN} = 0V to V _{CC}			2	μA
I _{LO}	Output leakage current	V _{OUT} = 0V to V _{CC}			10	μA
V _{OL1}	Output low voltage (open drain outputs, group 1 pins)	I _{OL} = 5mA			0.4	V
		I _{OL} = 1mA			0.4	
V _{OL2}	Output low voltage (group 2 pins)	V _{CC} = 5V, I _{OL} = 2.1mA			0.4	V
		V _{CC} < 4.5V, I _{OL} = 1mA			0.2	
V _{OH}	Output high voltage (group 2 pins)	V _{CC} = 5V, I _{OL} = -400mA	2.4			V
		V _{CC} < 4.5V, I _{OL} = -100mA	V _{CC} - 0.2			
V _{IL}	Input low voltage (group 2 pins)		-0.1		0.3 × V _{CC}	V
V _{IH}	Input high voltage (group 2 pins)		2		V _{CC} + 1	V
Analog Inputs						
V _{REFIN}	V _{REF} input voltage		1		5	V
V _{IN1}	Input voltage on V _{CC0} /CH0 through V _{CC3} /CH3		0		5.5	V
V _{IN2}	Input voltage on channels 4 through 7		0		2 × V _{REFIN}	V
V _{IN3}	Input voltage on OC0 through OC3		0		V _{CC}	V
I _{VRO}	V _{REFOUT} current	V _{REFOUT} = 2.5V				mA
		V _{REFOUT} = 2.048V				

Note 1: Unless otherwise specified V_{CC} is the highest of the four V_{CCX}/CHX inputs.



PIN DESCRIPTIONS

V_{CC0}/CH4 – V_{CC3}/CH7

These inputs are used as the voltage monitor inputs and the voltage supply for the SMD1108. Internally they are diode ORed and the input with the highest voltage potential will be the default supply voltage. For proper device operation at least one of the inputs must be at 2.7V or higher. Inputs CH0 to CH3 are monitored solely through the use of the ADC. V_{CC0}/CH4 to V_{CC3}/CH7 are also inputs to four programmable comparators. The under-voltage and over-voltage threshold voltage of each comparator is programmable.

V_{REFIN}

A reference voltage for the ADC. The user can select either the V_{REFIN} as the ADC reference or use the default internal reference voltage.

V_{REFOUT}

The internally generated reference voltage. It is programmable and can supply either 2.048V or 2.500V.

AGND, DGND, PGND, GND

These are the analog, digital, package, and common ground inputs, respectively.

AUXV_{CC}

AUXV_{CC} should be isolated from the system power supplies and tied to ground through capacitor C_{B/U}. During normal device operation C_{B/U} will be charged by the system supplies through the SMD1108. If system power is lost the charge on C_{B/U} will be used to store the status of the monitor inputs.

In the system environment AUXV_{CC} could also be connected to the front of the card (along with SDA and SCL and GND) so that power could be applied to the SMD1108 to read the contents of the NV status registers.

A0, A1 and A2

Address inputs. When addressing the SMD1108 either as a memory or an analog channel (or configuration register) the address inputs distinguish which one of eight possible devices sharing the common bus is being addressed.

CE#

A control mechanism for the 2-wire interface. The true state polarity is programmable. When driven true the interface is active and communications channels are open. When it is driven false all communications via the bus are disabled.

SDA

Serial data input/output pin. It should be tied to V_{CC} through a pull-up resistor.

SCL

Serial clock input pin. It should be tied to V_{CC} through a pull-up resistor.

CH0 to CH3

The analog channel inputs. These inputs are monitored solely through the use of the ADC.

OC0 to OC3

over-current sense inputs. They are paired with V_{CC0}/CH4 to V_{CC3}/CH7, respectively, and have a fixed 50mV offset with respect to their corresponding channel input.

MR#

An active low manual reset input. When MR# is driven low the reset output will immediately be driven low. MR# is not maskable and will always generate a reset sequence. The duration of the RST# pulse will be equal to the length of the MR# input pulse plus the programmed reset time-out period value.

WD_EN#

The watch dog and long dog enable input. It must be driven low to enable the operation of their respective timers. This can provide a convenient mechanism during “debug of code” or during a “power-on configuration” sequence.

WLDI

A manual watchdog timer input. A low to high transition on WDI will reset the watchdog and longdog timers. If the timer is not reset within the programmed period of time the SMD1108 will activate the WDO# output first and then the LDO# output.

RST#

An active low open drain output. It will be driven low by the programmed combination of V_{CC0}/CH4 to V_{CC3}/CH7 and/or MR# being driven low. RST# will stay low for the duration of the fault condition or the MR# low input and remain low for the duration of t_{PURST} after the removal of the fault condition or MR# returning high.



DLYD_RESET#

An active low open drain output. During normal system operation it will be driven low by the programmed combination of VCC0/CH4 to VCC3/CH7. During the power-on sequence it will be delayed to allow the system to power-up in a controlled sequenced order.

SMB_ALERT#

An active low open drain output. It will be driven low whenever one or more of the four auto-monitor inputs exceeds its limits. Once the SMB_ALERT# output is driven low the SMD1108 will respond to the industry standard SMB protocol and identify itself as the generator to the alert.

LIM_IRQ#

An active low open drain output that is programmable to be driven low whenever any one of the selected auto-monitor inputs exceeds the programmed high or low value.

FAULT

An open drain output that can be programmed to drive the output low whenever a selected source is out of limits (FAULT#). Conversely it can be programmed to drive the output low (FAULT) whenever the selected sources are within limits.

HEALTHY

An open drain output that can be programmed to drive the output low whenever a selected source is out of limits (HEALTHY). Conversely it can be programmed to drive the output low whenever the selected sources are within limits (HEALTHY#).

WDO#

Watchdog Timer Output is an active low open drain output that can be wire-ORed with any number of open drain outputs. Whenever the programmed time-out period of the watchdog timer is exceeded this output will be driven low.

LDO#

Longdog Timer Output is an active low open drain output that can be wire-ORed with any number of open drain outputs. Whenever the programmed time-out period of the longdog timer is exceeded this output will be driven low.

RDY#

An active low status output indicating the ADC has no conversion ongoing and the SMD1108 can be accessed via the serial interface without risk of disturbing a conversion.

GPO-0 to GPO-3

General purpose outputs that can be accessed via the two-wire serial interface. The register controlling these outputs is located in the GFS register section. The GPx outputs are open drain and will be active when a "1" is written to the corresponding bit position in GFS Register 0x98. The SMD1108 will power-up with the GPx bits cleared; therefore, the outputs will not be actively driven.

AUTOMON

This input must be high to enable the Auto Monitor function.

OV_IRQ#

This is an active low open drain output that is driven low when the selected over-voltage conditions are true.

OC_IRQ#

This is an active low open drain output that is driven low when the selected over-current conditions are true.

IRQ_RST#

Strobing this signal low will reset the IRQ# outputs.

UV_OVRD

Forcing this input high will disable over-Voltage reset conditions.

FAULT_IRQ#

This is an active low open drain output that is driven low when the selected fault conditions are true.



DEVICE OPERATION

THE ADC AND THE ANALOG SWITCH

10-bit ADC

The 10-bit ADC is a self-clocking SAR implementation. In the manual mode of conversion the sample and hold operation will begin after the SMD1108 has received the request for conversion and the channel address. See Table 1.

8 Analog Channels

The eight analog channels can be separated into two function blocks: the bottom four channels ($V_{CC0}/CH4$ to $V_{CC3}/CH7$) are primarily supply voltage monitors; the top four channels (CH0 to CH3) are primarily environmental monitors. All eight channels can be switched to the 10-bit ADC and have their inputs converted on-command. CH0 to CH3 may be placed in the Auto-Monitor mode.

$V_{CC0}/CH4$ to $V_{CC3}/CH7$ provide four inputs to the analog switch that controls the analog inputs to the ADC converter. Although these channels cannot be placed in the Auto-Monitor mode, the host can request a direct conversion.

Because these channels are designed to operate as supply voltage monitors they are each tied into a programmable comparator. The comparator threshold voltage is programmable and the polarity of the threshold is programmable. This allows very precise monitoring of under- or over-voltage conditions. Paired with each of these channels is an over-current input (OC0 to OC3) that is offset from its partner comparator by 50mV.

Signal to Noise ratio @ 25°C.		70dB mon.
THD		-80dB min.
Peak harmonic intermodulation distortion	2nd order	-80dB min.
	3rd order	-80dB min.
DC Accuracy		
Resolution		10 bits
Minimum resolution for which no missing codes are guaranteed		10 bits
Relative accuracy		$\pm 1/2$ LSB
DNL		± 1 LSB
Positive full scale error		± 2 LSB
Unpolar offset error	$V_{CC} = 5V$	± 2 LSB
	$V_{CC} = 2.7V$ to $3.6V$	
	$V_{CC} = 1.8V$ to $2.7V$	

2052 Table01 1.0

Table 1. Typical ADC Performance

TIMER FUNCTIONS

WATCHDOG and LONGDOG

The SMD1108 has two programmable watchdog timers each with its own output (WDO# and LDO#) and a common reset input (WLDI). Both are independently programmable and both can be placed in an idle mode. See Register 8C.

RST#

This reset output is intended to be used to drive the backend logic. It is an active low open drain output that is driven low whenever V_{CC0} , V_{CC1} , V_{CC2} or V_{CC3} is below its programmed threshold and/or MR# is being driven low. It will stay low for the duration of the fault condition or the MR# low input and remain low for the duration of t_{PURST} (the programmed reset pulse width) after removal of the fault condition or MR# returning high. It will also be driven low whenever an over-current condition is detected. See Register 8C.

DLYD_RST#

This output is activated by the same set of conditions as RST#. However, during a power-up operation it will not be immediately asserted. As soon as power to one of the $V_{CC0}/CH4$ to $V_{CC3}/CH7$ inputs is detected a time-out sequence will be started. The time-out period is programmable and should be equal to or greater than the worst case power-on skew between all the supplies being monitored. If all of the supplies have not reached their threshold before the time-out period, DLYD_RST# will be asserted. DLYD_RST# can then be used to disable a voltage sequencer such as the SMH4803A or SMH4804. See Register 8D.

OUTPUTS

FAULT and HEALTHY

Two programmable outputs (active high or active low) that will respond to programmed source activators. See Registers 8F and 90 through 95.

IRQs

The interrupt outputs are active low open drain outputs that are driven low whenever one of the corresponding monitor inputs senses an excursion beyond its programmed value. See Registers 88, 89, and 98 through 9F.

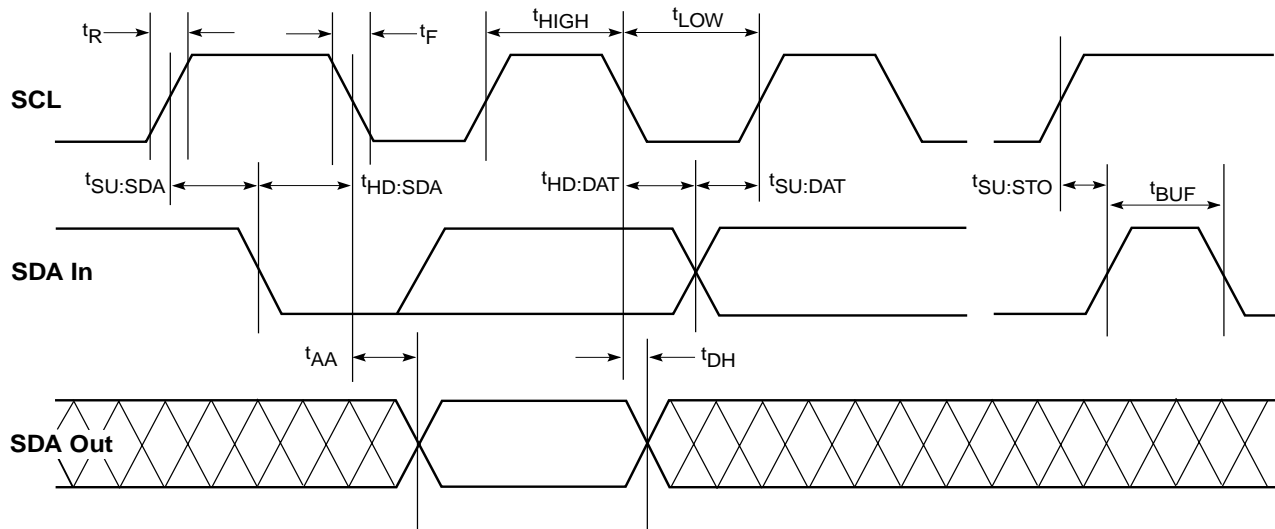


SERIAL INTERFACE

The SMD1108 has an industry standard 2-wire serial interface. It supports four (4) device-type addresses: 1010 for reading and writing the memory array; 1001 for reading and writing the nonvolatile limit registers and

initiating ADC conversions; 1011 for access to the configuration registers, and 0001 that is used for responses to the SMB_{ALERT} protocol

In order to facilitate host system presence detection techniques the SMD1108 provides A0, A1 and A2 address inputs.



2052 Fig01 1.0

Figure 1. Memory Timing

Symbol	Parameter	Conditions	Min.	Max.	Units
f_{SCL}	SCL clock frequency		0	100	kHz
t_{LOW}	Clock low period		4.7		μ s
t_{HIGH}	Clock high period		4.0		μ s
t_{BUF}	Bus free time	Before new transmission	4.7		μ s
$t_{SU:STA}$	Start condition setup time		4.7		μ s
$t_{HD:STA}$	Start condition hold time		4.0		μ s
$t_{SU:STO}$	Stop condition setup time		4.7		μ s
t_{AA}	Clock edge to valid output	SCL low to valid SDA (cycle n)	0.3	3.5	μ s
t_{DH}	Data Out hold time	SCL low (cycle n+1) to SDA change	0.3		μ s
t_R	SCL and SDA rise time			1000	ns
t_F	SCL and SDA fall time			300	ns
$t_{SU:DAT}$	Data In setup time		250		ns
$t_{HD:DAT}$	Data In hold time		0		ns
TI	Noise filter SCL and SDA	Noise suppression		100	ns
t_{WR}	Write cycle time			5	ms

2052 Table02 1.0

Table 2. Memory Timing



MEMORY AND REGISTER OPERATION

The SMD1108 incorporates a memory that is configured as a 128 x 8 array. Concatenated with the memory array are the sixteen registers that hold the upper and lower limits for ADC comparison tables. Additional registers provide space for configuration usage. Another space is provided for individual channel conversion initiations and reading the conversion data.

All read and write operations to memory are handled via an industry standard two-wire interface. The bus was designed for two-way, two-line serial communication between different integrated circuits. The two lines are a serial data line (SDA), and a serial clock line (SCL). The SDA line must be connected to a positive supply by a pull-up resistor, located somewhere on the bus

Input Data Protocol

The protocol defines any device that sends data onto the bus as a “transmitter” and any device that receives data as a “receiver.” The device controlling data transmission is called the “master” and the controlled device is called the “slave.” In all cases the SMD1108 will be a “slave” device since it never initiates any data transfers.

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during clock high time, because changes on the data line while SCL is high will be interpreted as start or stop condition.

START and STOP Conditions

When both the data and clock lines are high the bus is said to be not busy. A high-to-low transition on the data line, while the clock is high, is defined as the “START” condition. A low-to-high transition on the data line, while the clock is high, is defined as the “STOP” condition.

Acknowledge (ACK)

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either the master or the slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line low to ACKnowledge that it received the eight bits of data.

The SMD1108 will respond with an ACKnowledge after recognition of a START condition and its slave address byte. If both the device and a write operation are selected, the SMD1108 will respond with an ACKnowledge after the receipt of each subsequent 8-bit word. In the READ mode the SMD1108 transmits eight bits of data, then releases the SDA line, and monitors the line for an ACKnowledge

signal. If an ACKnowledge is detected, and no STOP condition is generated by the master, the SMD1108 will continue to transmit data. If an ACKnowledge is not detected the SMD1108 will terminate further data transmissions and await a STOP condition before returning to the standby power mode.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (DTI). For the SMD1108 the default memory DTI is 1010_{BIN}. The next three bits in the serial data stream are the device’s bus address. The bus address is assigned by biasing the A0, A1 and A2 pins into any one-of-eight unique addresses. The last bit of the data stream defines the operation to be performed. When set to “1” a read operation is selected; when set to “0” a write operation is selected.

MEMORY WRITE OPERATIONS

The SMD1108 allows two types of write operations: byte-write and page write. A byte-write operation writes a single byte during the nonvolatile write period (t_{WR}). The page write operation allows up to 16 bytes in the same page to be written during t_{WR} .

Byte Write

After the slave address is sent (to identify the slave device, and a read or write operation), a second byte is transmitted which contains the 8-bit address of any one of the 128 words in the array. Upon receipt of the word address the SMD1108 responds with an ACKnowledge. After receiving the next byte of data it again responds with an ACKnowledge. The master then terminates the transfer by generating a STOP condition, at which time the SMD1108 begins an internal write cycle. While the internal write cycle is in progress the SMD1108 inputs are disabled, and the device will not respond to any requests from the master.

Page Write

The SMD1108 is capable of a 16-byte page write operation. It is initiated in the same manner as the byte-write operation, but instead of terminating the write cycle after the first data word the master can transmit up to 15 more bytes of data. After the receipt of each byte the SMD1108 will respond with an ACKnowledge.



The SMD1108 automatically increments the address for subsequent data words. After the receipt of each word the low order address bits are internally incremented by one. The high order bits of the address byte remain constant. Should the master transmit more than 16 bytes, prior to generating the STOP condition, the address counter will "roll over," and the previously written data will be overwritten. As with the byte-write operation all inputs are disabled during the internal write cycle. Refer to Figure 2 for the address, ACKnowledge, and data transfer sequence.

Acknowledge Polling

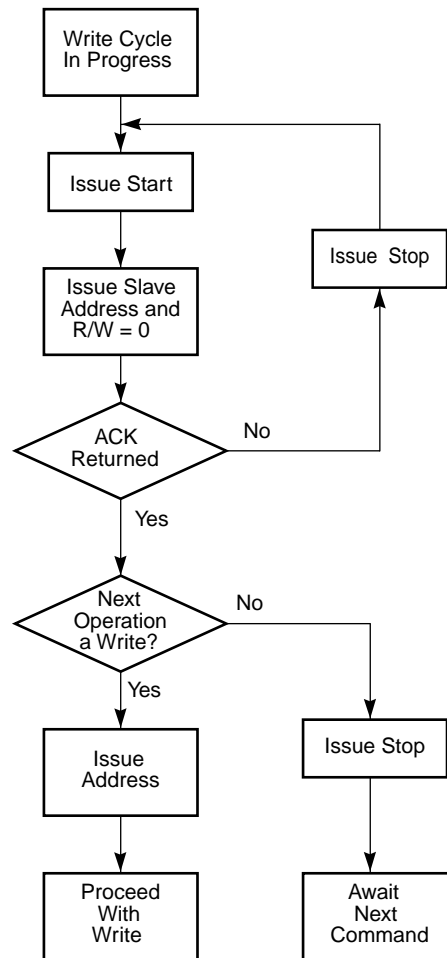
When the SMD1108 is performing an internal WRITE operation it will ignore any new START conditions. Since the device will only return an acknowledge after it accepts the START, the part can be continuously queried until an acknowledge is issued, indicating that the internal WRITE cycle is complete. See the flow diagram for the proper sequence of operations for polling.

READ OPERATIONS

Read operations are initiated with the R/W bit of the identification field set to "1." There are two different read options: (1) Current Address Byte Read; or (2) Random Address Byte Read

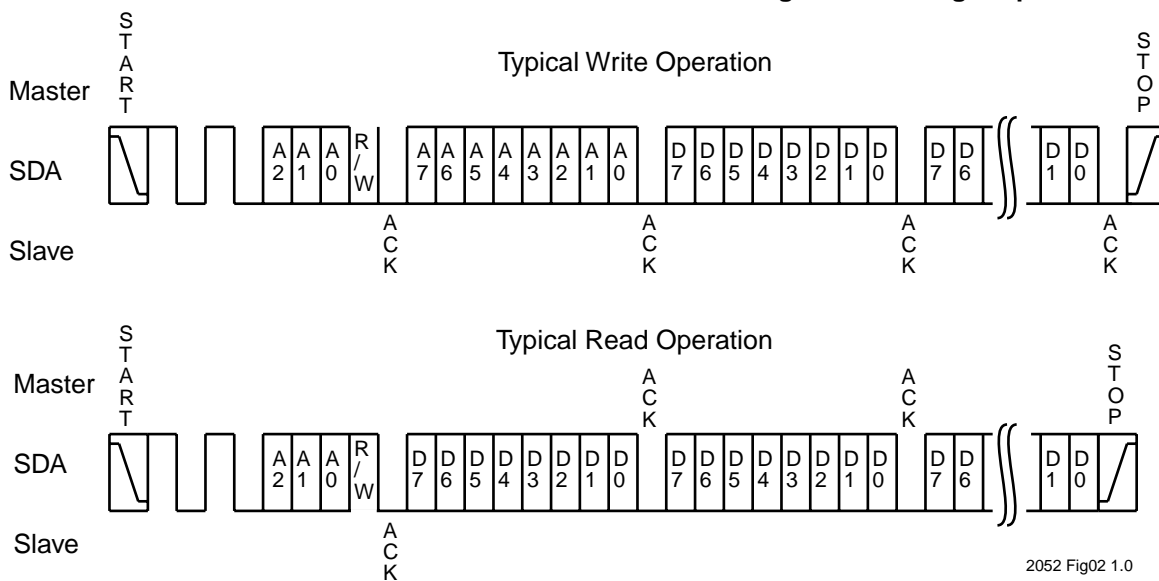
Current Address Read

The SMD1108 contains an internal address counter which maintains the address of the last word accessed, incremented by one. If the last address accessed (either a read



2052 Flow01 1.0

Figure 3. Polling Sequence



2052 Fig02 1.0

Figure 2. Address, Acknowledge and Data Transfer Sequence



or write) was to address location n, the next read operation would access data from address location n+1 and increment the current address pointer. When the SMD1108 receives the slave address field with the R/W bit set to "1" it issues an acknowledge and transmits the 8-bit word stored at address location n+1. The current address byte read operation only accesses a single byte of data. The master does not acknowledge the transfer, but does generate a stop condition. At this point, the SMD1108 discontinues data transmission.

Random Address Read

Random address read operations allow the master to access any memory location in a random fashion. This operation involves a two-step process. First, the master issues a write command which includes the start condition and the slave address field (with the R/W bit set to WRITE) followed by the address of the word it is to read. This procedure sets the internal address counter of the SMD1108 to the desired address. After the word address acknowledge is received by the master, the master immediately reissues a start condition followed by another slave address field with the R/W bit set to READ. The SMD1108 will respond with an acknowledge and then transmit the 8 data bits stored at the addressed location. At this point, the master does not acknowledge the transmission, but does generate the stop condition. The SMD1108 discontinues data transmission and reverts to its standby power mode.

Sequential READ

Sequential reads can be initiated as either a current address READ or random access READ. The first word is transmitted as with the other byte read modes (current address byte READ or random address byte READ). However, the master now responds with an ACKnowledge, indicating that it requires additional data from the

SMD1108. The SMD1108 continues to output data for each ACKnowledge received. The master terminates the sequential READ operation by not responding with an ACKnowledge, and issues a STOP conditions. During a sequential read operation the internal address counter is automatically incremented with each ACKnowledge signal. For read operations all address bits are incremented, allowing the entire array to be read using a single read command. After a count of the last memory address the address counter will 'roll-over' and the memory will continue to output data.

SMB_{ALERT}

The function of the SMB_{ALERT} output is similar to a standard interrupt. Whenever one of the selected channels exceeds its limits the SMB_{ALERT} pin will be driven low. This action begins an exchange of information across the 2-wire interface that establishes the source of the interrupt.

As shown in Figure 4 SMB_{ALERT} drives low and the host responds with the Alert Response Address [0001 1001]. The SMD1108 will issue an acknowledge and then output its address, starting with the device type identifier for the PSF registers [1001]. Following this the SMD1108 outputs its bus address reflecting the biasing of the A0, A1 and A2 pins. If the response to any bus address option is selected and the pins are not biased the read back will be [111]. The last bit is undefined.

At this point the Host should not issue an ACK, but immediately generate a stop condition. The SMD1108 will continue driving the SMB_{ALERT} output low until the Host responds back by generating a start condition followed by the SMD1108 address. The SMD1108 will generate an ACK and release the SMB_{ALERT} pin.

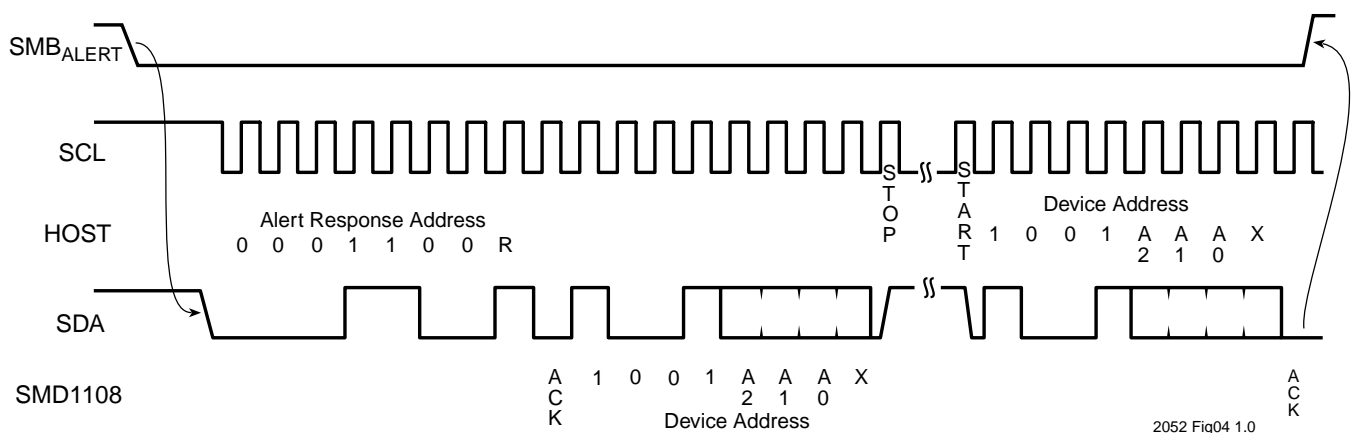


Figure 4. SMB_{ALERT} Sequence



REGISTERS

REGISTER READ/WRITE

The registers are read and written using the same 2-wire bus as the memory. The configuration registers and the GFS Registers are written as shown in Figure 5. Reads of the registers must be executed like a random read operation. That is; a dummy write must be issued in order to set the address pointer for the following read.

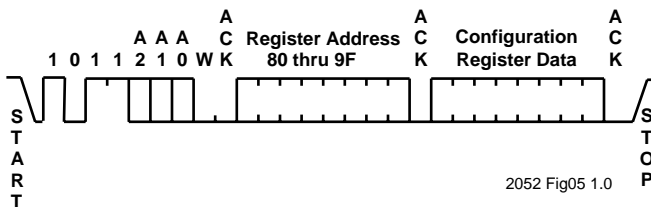


Figure 5. Writing to the Configuration Registers

The limits registers for channels 0 through 3 are located at the top of the ADC address space and utilize the 1001 DTI. Unlike the configuration registers that are limited to single byte writes or reads, the ADC limit registers can be written in page mode. The example in Figure 6 shows two byte writes to configure the CH0 Lower Limit.

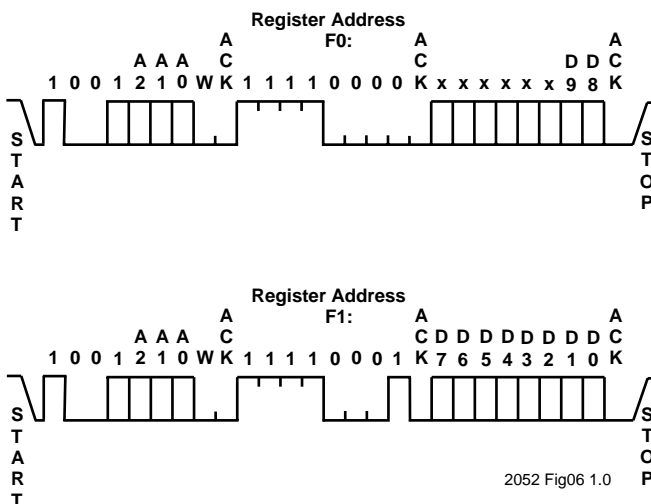


Figure 6. Writing to the Limits Registers

Even though the ADC cannot be written, performing commanded conversions (non-auto-monitor mode) requires a dummy write operation to select the proper channel and indicate the type of conversion process that is being requested. The sequence would be: address the device using 1001 as the DTI followed by the bus address and a write bit. The next byte contains the conversion process requested and the channel or channel group to be converted.

Single Channel Conversion

The single channel read allows the host to perform manual conversions on a single channel. The state of bits CH2, CH1 and CH0 selects one-of-eight channels. Reading DTI 1001 will return the converted data. If the host continues clocking SCL without an interim stop command the SMD1108 will continue conversions on the selected channel and output the data as clocked. See the timing sequence diagrams in Figure 7.

Multi-Channel Conversion: 4

Command 001 will configure the channel conversion such that the MUX will switch channels 0 through 3 sequentially.

Multi-Channel Conversion: 8

Command 011 will configure the channel conversion such that the MUX will switch channels 0 through 7 sequentially.

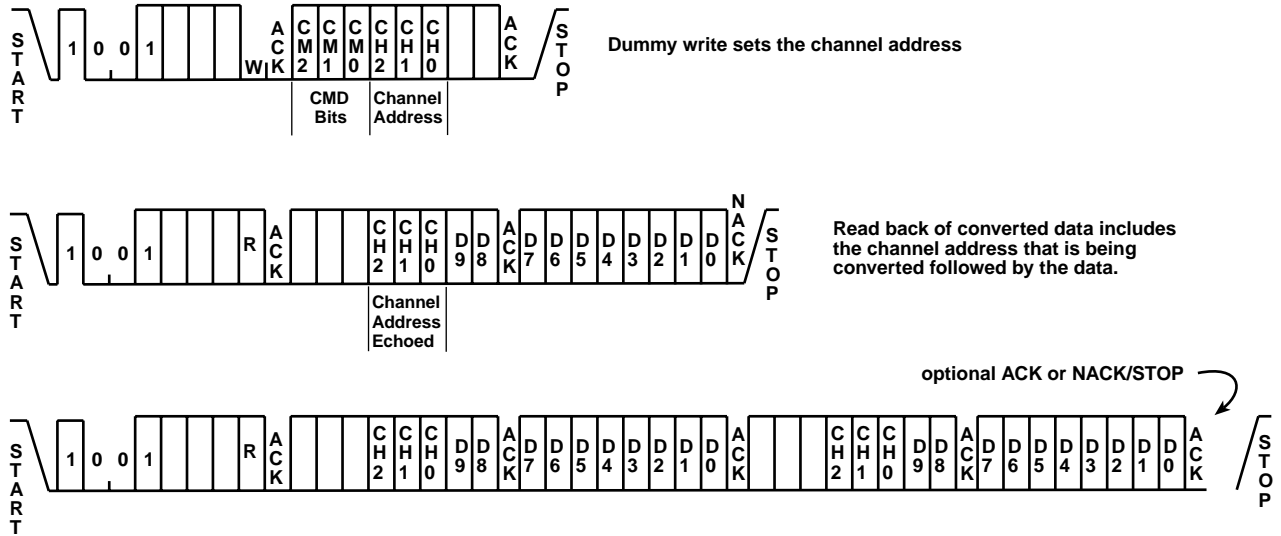
Differential Conversion

In order to provide a very accurate current sense the SMD1108 can perform a differential conversion on the select CHx/OCx input combination. This is limited to channels 4 through 7 and their corresponding OC inputs.

7	6	5	4	3	2	1	0	Bit
CMD			CH2	CH1	CH0	x	x	Function
0	0	0	CH2	CH1	CH0			Single channel read mode
0	0	1	x					Continuous read mode 1
0	1	1	x					Continuous read mode 2
1	0	0	1	CH1	CH0			Differential conversion

Table 3. Command/Address Byte

2052 Table03 1.0



In a continuous read mode the SMD1108 will clock data out as shown above repeating the channel address for each conversion that takes place. For the multi-channel conversions the channel numbers increment, e.g., n to n+1.

2052 Fig07 1.0

Figure 7. Continuous Read

M-ADD	MSB						LSB	Function	
F0	x	x	x	x	x	x	D9	D8	Channel #0 low limit
F1	D7	D6	D5	D4	D3	D2	D1	D0	Channel #0 low limit
F2	x	x	x	x	x	x	D9	D8	Channel #0 high limit
F3	D7	D6	D5	D4	D3	D2	D1	D0	Channel #0 high limit
F4	x	x	x	x	x	x	D9	D8	Channel #1 low limit
F5	D7	D6	D5	D4	D3	D2	D1	D0	Channel #1 low limit
F6	x	x	x	x	x	x	D9	D8	Channel #1 high limit
F7	D7	D6	D5	D4	D3	D2	D1	D0	Channel #1 high limit
F8	x	x	x	x	x	x	D9	D8	Channel #2 low limit
F9	D7	D6	D5	D4	D3	D2	D1	D0	Channel #2 low limit
FA	x	x	x	x	x	x	D9	D8	Channel #2 high limit
FB	D7	D6	D5	D4	D3	D2	D1	D0	Channel #2 high limit
FC	x	x	x	x	x	x	D9	D8	Channel #3 low limit
FD	D7	D6	D5	D4	D3	D2	D1	D0	Channel #3 low limit
FE	x	x	x	x	x	x	D9	D8	Channel #3 high limit
FF	D7	D6	D5	D4	D3	D2	D1	D0	Channel #3 high limit

2052 Table04 1.0

Table 4. ADC Registers Located at the Top of 1001 Address Space



REGISTER PARTITIONING

The registers have been divided into two main functional blocks. The Configuration registers (from 0x80 through 0x95) are the primary setup registers that define the SMD1108 for its specific application. These registers can

be (1) left open for read and write operations, (2) locked for writes but open for reads, or (3) totally blocked so that they cannot be read or written.

The balance of the registers (the GSF registers) will frequently be used during system operation; therefore, the lock combinations are more flexible. They can be (1) locked for read and writes, (2) open for read and writes but excluding the configuration registers, (3) read all registers but write GSF only, or (4) read and write all registers.

The organization, bit patterns and functions of the registers are illustrated in Tables 6 through 33.

Registers 80 through 83 set the under-voltage threshold for the selected channel: CH4 through CH7. The register value is determined by subtracting 0.9V from the desired threshold, dividing the result by 0.02 and converting that to a hexadecimal value.

The formula is $(UV_{TH} - 0.9) / 0.02 = \text{Decimal value (convert to hexadecimal)}$.

For example, if the UV threshold is to be 4.6V:
 $(4.6 - 0.9) / 0.02 = 185_{DEC} = B9_{HEX}$

Reg. #	Reg. Name	Reg. Type
80	Channel configuration	Configuration Registers
81		
82		
83		
84		
85		
86		
87		
88		
89		
8A	Address configuration	Configuration Registers
8B	V _{REF} configuration	
8C	Timers 1	
8D	Timers 2	
8E	Quick trip	
8F	Healthy/Fault configuration	
90	Healthy pin configuration	
91	Healthy pin configuration	
92	Fault pin configuration	
93	Fault pin configuration	
94	Fault mask	GFS Register
95	Fault mask	
96	Reserved	
97	Reserved	
98	GPO register	
99	Software reset	
9A	Status register	
9B	Status register	
9C	Reserved	
9D	Reserved	
9E	Fault latch	GFS Register
9F	Fault latch	

2052 Table05 1.0

Table 5. Register Address Map



7	6	5	4	3	2	1	0	Function
Ref7	Ref6	Ref5	Ref4	Ref3	Ref2	Ref1	Ref0	Reference voltage for $V_{CC0}/CH4$

2052 Table06 1.0

Table 6. Register 80 $V_{CC0}/CH4$ UV Threshold

7	6	5	4	3	2	1	0	Function
Ref7	Ref6	Ref5	Ref4	Ref3	Ref2	Ref1	Ref0	Reference voltage for $V_{CC1}/CH5$

2052 Table07 1.0

Table 7. Register 81 $V_{CC1}/CH5$ UV Threshold

7	6	5	4	3	2	1	0	Function
Ref7	Ref6	Ref5	Ref4	Ref3	Ref2	Ref1	Ref0	Reference voltage for $V_{CC2}/CH6$

2052 Table08 1.0

Table 8. Register 82 $V_{CC2}/CH6$ UV Threshold

7	6	5	4	3	2	1	0	Function
Ref7	Ref6	Ref5	Ref4	Ref3	Ref2	Ref1	Ref0	Reference voltage for $V_{CC3}/CH7$

2052 Table09 1.0

Table 9. Register 83 $V_{CC3}/CH7$ UV Threshold

Registers 84 through 87 set the over-voltage threshold for the selected channel: CH4 through CH7. The OV threshold minimum is equal to 120% of the channel's UV threshold. An offset of as much as 244% of the UV threshold is possible.

The formula is $[OV_{TH} - (UV_{TH} \times 1.2)] / (UV_{TH} \times 0.04) =$ Decimal value (convert to hexadecimal).

The maximum register value would be $31_{DEC} = 1F_{HEX}$.

7	6	5	4	3	2	1	0	Function
x	x	x	OV4	OV3	OV2	OV1	OV0	Over-voltage offset for $V_{CC0}/CH4$

2052 Table10 1.0

Table 10. Register 84 $V_{CC0}/CH4$ OV Threshold

7	6	5	4	3	2	1	0	Function
x	x	x	OV4	OV3	OV2	OV1	OV0	Over-voltage offset for $V_{CC1}/CH5$

2052 Table11 1.0

Table 11. Register 85 $V_{CC1}/CH5$ OV Threshold

7	6	5	4	3	2	1	0	Function
x	x	x	OV4	OV3	OV2	OV1	OV0	Over-voltage offset for $V_{CC2}/CH6$

2052 Table12 1.0

Table 12. Register 86 $V_{CC2}/CH6$ OV Threshold

7	6	5	4	3	2	1	0	Function
x	x	x	OV4	OV3	OV2	OV1	OV0	Over-voltage offset for $V_{CC3}/CH7$

2052 Table13 1.0

Table 13. Register 87 $V_{CC3}/CH7$ OV Threshold



Registers 88 and 89 provide selective enabling of the channels and the channels' functions. When channels 0 through 3 are enabled any out-of-limit condition will activate the LIM_IRQ# and SMB_{ALERT}# outputs. Channels 4 through 7 are more complex in that they are inputs to three

instant action measurements: under-voltage, over-voltage and over-current. Each one of these measurements can be enabled on a channel by channel basis to activate one of the three potential output reactions.

7	6	5	4	3	2	1	0	Function
x	x	x	x	UV3 (CH7)	UV2 (CH6)	UV1 (CH5)	UV0 (CH4)	A "1" enables the channel; an UV condition will cause a RESET.
OV3 (CH7)	OV2 (CH6)	OV1 (CH5)	OV0 (CH4)	x	x	x	x	A "1" enables the channel; an OV condition will cause an OV_IRQ.

2052 Table14 1.0

Table 14. Register 88 Channel Enable — Part 1

7	6	5	4	3	2	1	0	Function
x	x	x	x	LIM3 (CH7)	LIM2 (CH6)	LIM1 (CH5)	LIM0 (CH4)	A "1" enables the channel; an out-of-limit condition will cause a LM_IRQ# and a SMB _{ALERT} .
OC3 (CH7)	OC2 (CH6)	OC1 (CH5)	OC0 (CH4)	x	x	x	x	A "1" enables the channel; an over-current condition will cause an OC_IRQ#.

2052 Table15 1.0

Table 15. Register 89 Channel Enable — Part 2

Register 8A controls access to the SMD1108 with regard to the 2-wire interface and the function blocks that are accessed through the 2-wire bus.

7	6	5	4	3	2	1	0	Bits
Reg. Access		ACK	Device Type	Device Address	CE	x	x	Function
x	x	x	x	x	0	x	x	CE# input active low
				x	1	x	x	CE# input active high
				0	x	x	x	Responds to address pin biased address only
				1	x	x	x	Responds to any bus address
			0	x	x	x	x	EEPROM responds to 1010
			1	x	x	x	x	EEPROM responds to 1110
			0	x	x	x	x	ACK and access to DTI 1010
			1	x	x	x	x	No ACK/ no access to DTI 1010
0	0	x	x	x	x	x	All registers locked: no read, no write	
0	1	x	x	x	x	x	Read and write GFS registers only (98 through 9F). All configuration registers locked.	
1	0	x	x	x	x	x	Read all registers. Write GFS registers.	
1	1	x	x	x	x	x	Read and write all registers	

2052 Table16 1.0

2052 Table16 1.0

Table 16. Register 8A Slave Address Configuration



Register 8B controls the source for the ADC's reference, optional over-current trip values, and channel 3 vs. temp sense enable.

7	6	5	4	3	2	1	0	Bits				
V_{REF} SOURCE		Reserved		?	NVFL	OC	V_{REF}	Function				
x	x	x	x	x	x	x	0	V _{REF} = 2.048V				
							1	V _{REF} = 2.500V				
						0	x	Over-current trip = 25mV				
						1	x	Over-current trip = 50mV				
					0	x	x	x	Disable non-volatile fault latch			
					1	x	x	x	Enable non-volatile fault latch			
					0	x	x	x	Disable temp sensor			
					1	x	x	x	Enable temp sensor (vs. Channel 3)			
					0	0	x	x	x	x	x	Reserved function. Set to 0.
					0	1	x	x	x	x	x	Reserved function. Set to 0.
0	0	x	x	x	x	x	Use internally generated V _{REF}					
0	1	x	x	x	x	x	Reserved					
1	0	x	x	x	x	x	Reserved					
1	1	x	x	x	x	x	Use V _{REF} input					

2052 Table17 1.0

Table 17. Register 8B Configuration

7	6	5	4	3	2	1	0	Bits
PRT1	PRT0	LD2	LD1	LD0	WD2	WD1	WD0	Function
x	x	x	x	x	0	0	0	Watch dog timer disabled
					0	0	1	400ms Watch dog timer interval
					0	1	0	800ms Watch dog timer interval
					0	1	1	1600ms Watch dog timer interval
					1	0	0	3200ms Watch dog timer interval
		0	0	0	x	x	x	Long dog timer disabled
		0	0	1	x	x	x	800ms Long dog timer interval
		0	1	0	x	x	x	1600ms Long dog timer interval
		0	1	1	x	x	x	3200ms Long dog timer interval
		1	0	0	x	x	x	6400ms Long dog timer interval
0	0	x	x	x	x	x	25ms Reset interval	
0	1	x	x	x	x	x	50ms Reset interval	
1	0	x	x	x	x	x	100ms Reset interval	
1	1	x	x	x	x	x	200ms Reset interval	

2052 Table18 1.0

Table 18. Register 8C Reset Pulse Width and Timer Delays



Register 8D controls three delays. DRT2, DRT1, and DRT0 control the hold-off time period for generation of any IRQ output and define the hold-off for the DLYD_RST# output. OCD1 and OCD0 define the delay from the first

sensing of an over-current condition, and how long that condition exists before taking action. FWD1 and FWD0 control the hold-off period from the first sensing of a fault condition until recording all active conditions.

7	6	5	4	3	2	1	0	Bits		
FWD1	FWD0	OCD1	OCD0	x	DRT2	DRT1	DRT0	Function		
x	x	x	x	x	0	x	x	Delayed reset timer disabled		
					1	0	0	200ms Delayed reset timer interval		
					1	0	1	400ms Delayed reset timer interval		
					1	1	0	800ms Delayed reset timer interval		
					1	1	1	1600ms Delayed reset timer interval		
		0	0		0	25µs Over-current trip delay				
		0	1		1	50µs Over-current trip delay				
		1	0		0	100µs Over-current trip delay				
		1	1		1	200µs Over-current trip delay				
		0	0		x	x	x	x	x	Fault write sense delay off
		0	1		x	x	x	x	x	50µs Fault write sense delay
		1	0		x	x	x	x	x	100µs Fault write sense delay
1	1	x	x	x	x	x	200µs Fault write sense delay			

2052 Table19 1.0

Table 19. Register 8D Reset Pulse Width and Timer Delays



Register 8E selects the QuickTrip thresholds. The thresholds are interrelated with the value of the internal V_{REF} controlled by the state of bit 1 in Register 8B.

7	6	5	4	3	2	1	0	Bits		
QT1 CH4	QT0 CH4	QT1 CH5	QT0 CH5	QT1 CH6	QT0 CH6	QT1 CH7	QT0 CH7	Function: QT threshold		
x	x	x	x	x	x	0	0	Off		
						0	1	50mV/75mV		
						1	0	75mV/100mV		
						1	1	125mV/150mV		
		0	0	0	1	x	x	x	x	Off
								0	1	50mV/75mV
								1	0	75mV/100mV
								1	1	125mV/150mV
		0	1	0	0	x	x	x	x	Off
				0	1	x	x	x	x	50mV/75mV
				1	0	x	x	x	x	75mV/100mV
				1	1	x	x	x	x	125mV/150mV
0	0	x	x	x	x	x	x	Off		
0	1	x	x	x	x	x	x	50mV/75mV		
1	0	x	x	x	x	x	x	75mV/100mV		
1	1	x	x	x	x	x	x	125mV/150mV		

2052 Table20 1.0

Table 20. Register 8E Quick Trip Thresholds



Register 8F controls the function of the HEALTHY and FAULT outputs and the conditions that can drive them.

7	6	5	4	3	2	1	0	Bits					
Healthy & Fault	UV_OVRD#	FAULT Reset	FAULT Latch	FAULT State	HEALTHY Reset	HEALTHY Latch	HEALTHY State	Function					
x	x	x	x	x	x	x	0	HEALTHY output low					
							1	HEALTHY output high					
						0	x	Do not latch HEALTHY					
						1	x	Latch HEALTHY					
					0	x	x	x	x	x	x	x	HEALTHY unaffected by reset
													HEALTHY goes false on reset
					0	x	x	x	x	x	x	x	FAULT output active low
													FAULT output active high
					0	x	x	x	x	x	x	x	Do not latch FAULT
													Latch FAULT
					0	x	x	x	x	x	x	x	FAULT unaffected by reset
													FAULT goes true on reset
					0	x	x	x	x	x	x	x	UV_OVRD# will override FAULT conditions
					1	x	x	x	x	x	x	x	HEALTHY & FAULT ignore UV_OVRD#
0	x	x	x	x	x	x	x	Enabled channels affect HEALTHY & FAULT					
1	x	x	x	x	x	x	x	Disabled channels affect HEALTHY & FAULT					

2052 Table21 1.0

Table 21. Register 8F HEALTHY and FAULT Output Control



Registers 90 through 93 control the sources of activation for the HEALTHY and FAULT outputs. For the HEALTHY output to be true all the selected sources must be within their limits. This is effectively an ANDing function. For the

FAULT output to be true only one of the selected sources need be out of limits (ORing). If the same sources for HEALTHY and FAULT are selected then only one of the two outputs can be true at one time.

7	6	5	4	3	2	1	0	Bit
OV3 CH7	OV2 CH6	OV1 CH5	OV0 CH4	UV3 CH7	UV2 CH6	UV1 CH5	UV0 CH4	Function
0	0	0	0	0	0	0	0	HEALTHY signal unaffected by condition
1	1	1	1	1	1	1	1	HEALTHY signal goes false on condition

2052 Table22 1.0

Table 22. Register 90 HEALTHY Deactivation Sources

7	6	5	4	3	2	1	0	Bit
OC3 CH7	OC2 CH6	OC1 CH5	OC0 CH4	LIM3 CH3	LIM2 CH2	LIM1 CH1	LIM0 CH0	Function
0	0	0	0	0	0	0	0	HEALTHY signal unaffected by condition
1	1	1	1	1	1	1	1	HEALTHY signal goes false on condition

2052 Table23 1.0

Table 23. Register 91 HEALTHY Deactivation Sources

7	6	5	4	3	2	1	0	Bit
OV3 CH7	OV2 CH6	OV1 CH5	OV0 CH4	UV3 CH7	UV2 CH6	UV1 CH5	UV0 CH4	Function
0	0	0	0	0	0	0	0	FAULT signal unaffected by condition
1	1	1	1	1	1	1	1	FAULT signal goes true on condition

2052 Table24 1.0

Table 24. Register 92 FAULT Activation Sources

7	6	5	4	3	2	1	0	Bit
OC3 CH7	OC2 CH6	OC1 CH5	OC0 CH4	LIM3 CH3	LIM2 CH2	LIM1 CH1	LIM0 CH0	Function
0	0	0	0	0	0	0	0	FAULT signal unaffected by condition
1	1	1	1	1	1	1	1	FAULT signal goes false on condition

2052 Table25 1.0

Table 25. Register 93 FAULT Activation Sources



Registers 94 & 95 are similar to FAULT registers 92 and 93. If any one of the selected sources is true the fault condition will be recorded in the nonvolatile fault latches 9E and 9F. This in turn will drive the FLT_IRQ# output low.

7	6	5	4	3	2	1	0	Bit
OV3 CH7	OV2 CH6	OV1 CH5	OV0 CH4	UV3 CH7	UV2 CH6	UV1 CH5	UV0 CH4	Function
0	0	0	0	0	0	0	0	FAULT latch unaffected by condition
1	1	1	1	1	1	1	1	FAULT latch records out of limit condition

2052 Table26 1.0

Table 26. Register 94 FAULT Latch Mask

7	6	5	4	3	2	1	0	Bit
OC3 CH7	OC2 CH6	OC1 CH5	OC0 CH4	LIM3 CH3	LIM2 CH2	LIM1 CH1	LIM0 CH0	Function
0	0	0	0	0	0	0	0	FAULT latch unaffected by condition
1	1	1	1	1	1	1	1	FAULT latch records out of limit condition

2052 Table27 1.0

Table 27. Register 95 FAULT Latch Mask

THE GFS REGISTERS

The balance of the registers can be thought of as the operation registers. That is, the previous registers define

the part's function and their contents will most likely be written once and never altered. The following GPO, fault, and status registers will be actively read and written during the system operation.

7	6	5	4	3	2	1	0	Bit
x	x	x	x	GPO3	GPO2	GPO1	GPO0	Function
				0	0	0	0	Power on state — non-active
				1	1	1	1	Corresponding output to ground

2052 Table28 1.0

Table 28. GFS Register 98 GPO Output Control

Register 99 provides a software method for activating a RESET output or clearing an IRQ (this effectively mimics the IRQ_RST# input).

7	6	5	4	3	2	1	0	Bit
Reserved						Soft Reset	Clear IRQ	Function
0	0	0	0	0	0	x	1	Clears any IRQ except FLT_IRQ#
						1	x	Starts reset cycle, then self clears

2052 Table29 1.0

Table 29. GFS Register 99 GPO Output Control



Registers 9A and 9B are the status registers. These registers are read-only and are volatile. The Status Register is cleared by forcing the IRQ_RST# input low.

7	6	5	4	3	2	1	0	Bit
OV3 CH7	OV2 CH6	OV1 CH5	OV0 CH4	UV3 CH7	UV2 CH6	UV1 CH5	UV0 CH4	Function
0	0	0	0	0	0	0	0	Condition not the cause of an IRQ
1	1	1	1	1	1	1	1	Condition the cause of an IRQ

2052 Table30 1.0

Table 30. GFS Register 9A Status Register (Read Only)

7	6	5	4	3	2	1	0	Bit
OC3 CH7	OC2 CH6	OC1 CH5	OC0 CH4	LIM3 CH3	LIM2 CH2	LIM1 CH1	LIM0 CH0	Function
0	0	0	0	0	0	0	0	Condition not the cause of an IRQ
1	1	1	1	1	1	1	1	Condition the cause of an IRQ

2052 Table31 1.0

Table 31. GFS Register 9B Status Register (Read Only)

Registers 9E and 9F are the Fault registers. These registers are nonvolatile and can only be cleared by writing to the affected bit. This register is cleared by writing a 0 to the affected bit location.

7	6	5	4	3	2	1	0	Bit
OV3 CH7	OV2 CH6	OV1 CH5	OV0 CH4	UV3 CH7	UV2 CH6	UV1 CH5	UV0 CH4	Function
0	0	0	0	0	0	0	0	Condition not the cause of an IRQ
1	1	1	1	1	1	1	1	Condition the cause of an IRQ

2052 Table32 1.0

Table 32. GFS Register 9E NV Fault Latch

7	6	5	4	3	2	1	0	Bit
OC3 CH7	OC2 CH6	OC1 CH5	OC0 CH4	LIM3 CH3	LIM2 CH2	LIM1 CH1	LIM0 CH0	Function
0	0	0	0	0	0	0	0	Condition not the cause of an IRQ
1	1	1	1	1	1	1	1	Condition the cause of an IRQ

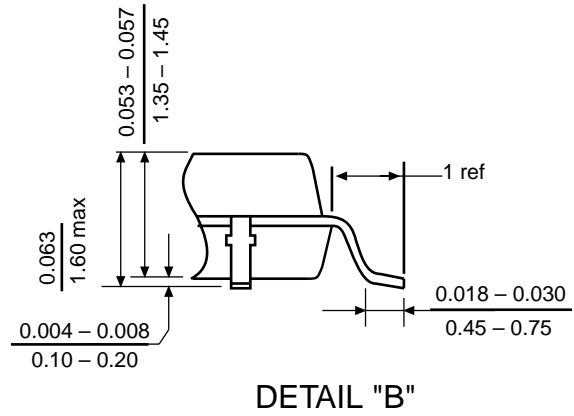
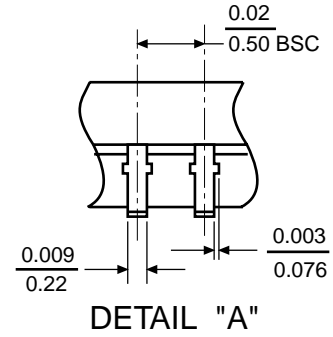
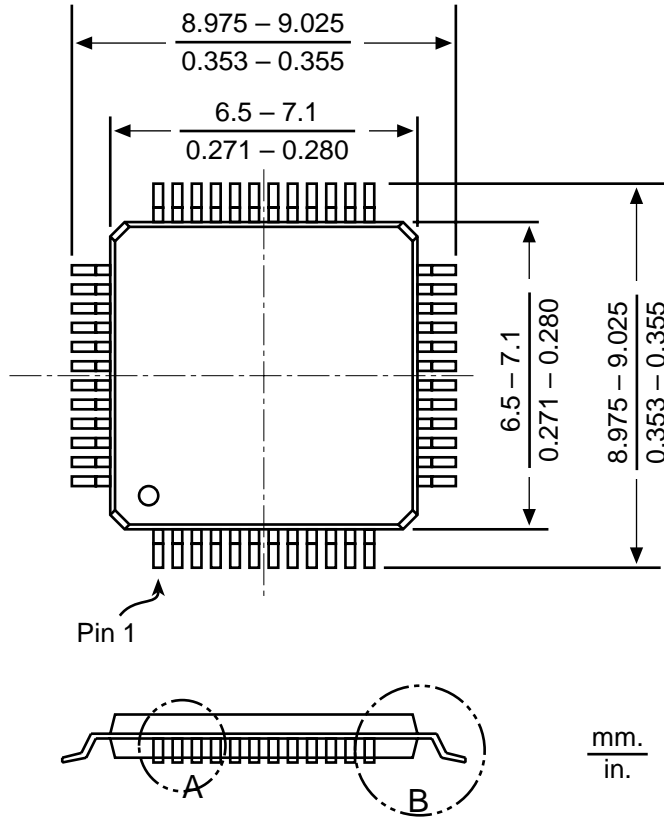
2052 Table33 1.0

Table 33. GFS Register 9F NV Fault Latch



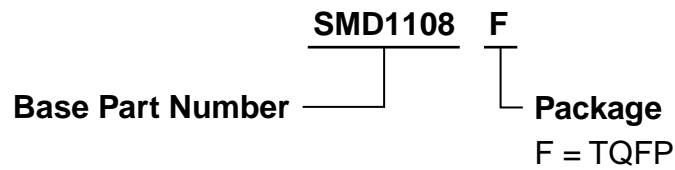
PACKAGE

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