

# 4 Megabit ROM + 256 Kilobit SRAM ROM/RAM Combo

## SST30VR043



Data Sheet

### FEATURES:

- **Organized as 512K x8 ROM + 32K x8 SRAM**
- **ROM/RAM combo on a monolithic chip**
- **Wide Operating Voltage Range: 2.7-3.3V**
- **Chip Access Time**
  - 2.7V Operation: 500 ns (Max.)
- **Low Power Dissipation:**
  - Standby  
3.0V Operation: 1.0 $\mu$ W (Typical)
  - Operating  
3.0V Operation: 3.0 mW (Typical)
- **Fully Static Operation**
  - No clock or refresh required
- **Three state Outputs**
- **Packages Available**
  - 32-Pin TSOP (8mm x 20mm)
  - 32-Pin STSOP (8mm x 13.4mm)

### PRODUCT DESCRIPTION

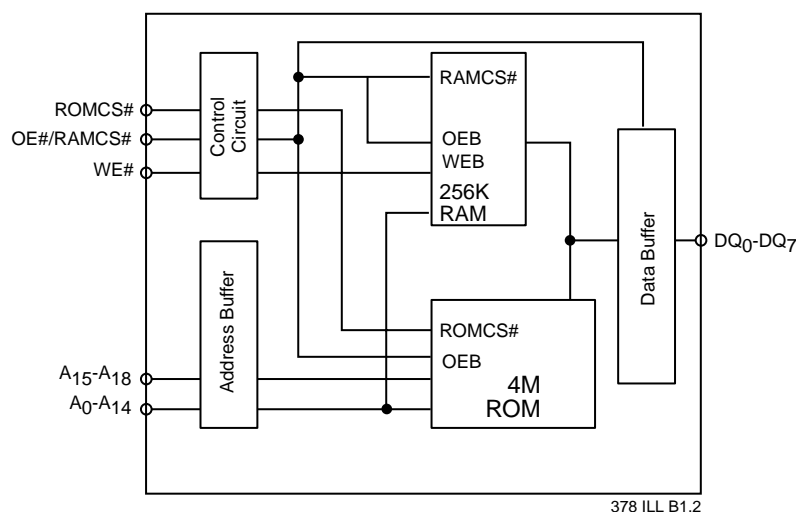
The SST30VR043 is a ROM/RAM combo chip consisting of 4 Mbit Read Only Memory organized as 512 KBytes and a 256 Kbit Static Random Access Memory organized as 32 KBytes. Output Enable Input (OE#) is pin-shared with RAMCS# (RAM Enable Input) signal in order to maintain the standard 32 pin TSOP package.

The device is fabricated using SST's advanced CMOS low power process technology.

The SST30VR043 has an output enable input for precise control of the data outputs. It also has two (2) separate chip enable inputs for selection of either RAM or ROM and minimize current drain during power-down mode.

The SST30VR043 is particularly well suited for use in low voltage (2.7-3.3V) operation such as pagers, organizers and other handheld applications.

### FUNCTIONAL BLOCK DIAGRAM OF SST30VR043 ROM/RAM COMBO





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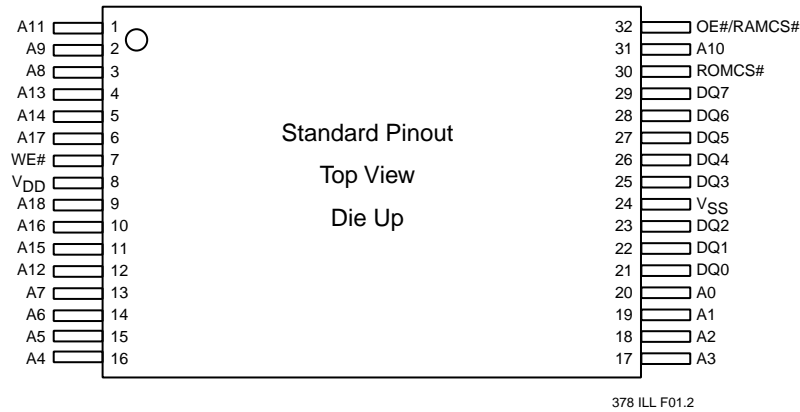


FIGURE 1: PIN ASSIGNMENTS

TABLE 1: PIN DESCRIPTION

Symbol	Pin Name
A <sub>0</sub> -A <sub>18</sub>	Address Inputs
WE#	Write Enable Input
OE#/RAMCS#	Output Enable/RAM Enable Input
ROMCS#	ROM Enable Input
DQ <sub>0</sub> -DQ <sub>7</sub>	Data Inputs/Outputs
V <sub>DD</sub>	Power Supply
V <sub>SS</sub>	Ground

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**Absolute Maximum Stress Ratings** (Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Voltage on Any Pin Relative to V <sub>SS</sub> .....	-0.5V to V <sub>DD</sub> + 0.5V
Voltage on V <sub>DD</sub> Supply Relative to V <sub>SS</sub> .....	-0.5 to 4.0V
Power Dissipation .....	1.0W
Storage Temperature .....	-65°C to +150°C
Operating Temperature .....	-20°C to +70°C
Soldering Temperature (10 Seconds Lead Only) .....	260°C

## OPERATING RANGE

Range	Ambient Temp	V <sub>DD</sub>
Commercial	0 °C to +70 °C	2.7-3.3V
Extended	-20 °C to +70 °C	2.7-3.3V
Industrial	-40 °C to +85 °C	2.7-3.3V

## AC CONDITIONS OF TEST

Input Pulse Level .....	0-3V
Input & Output Timing Reference Levels .....	1.5V
Input Rise/Fall Time .....	5 ns
Output Load .....	C <sub>L</sub> = 100 pF



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**TABLE 2: RECOMMENDED DC OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Units
V <sub>DD</sub>	Supply Voltage	2.7	3.3	V
V <sub>SS</sub>	Ground	0	0	V
V <sub>IH</sub>	Input High Voltage	2.4	V <sub>DD</sub> +0.5	V
V <sub>IL</sub>	Input Low Voltage	-0.3	0.3	V

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**TABLE 3: DC OPERATING CHARACTERISTICS**

Symbol	Parameter	V <sub>DD</sub> = 3.0±0.3V			Test Conditions
		Min	Max	Units	
I <sub>LI</sub>	Input Leakage Current	-1	1	μA	V <sub>IN</sub> = V <sub>SS</sub> to V <sub>DD</sub>
I <sub>LO</sub>	Output Leakage Current	-1	1	μA	ROMCS# = RAMCS# = V <sub>IH</sub> or OE# = V <sub>IH</sub> or WE# = V <sub>IL</sub> , V <sub>I/O</sub> = V <sub>SS</sub> to V <sub>DD</sub>
I <sub>DD1</sub>	ROM Operating Supply Current		4.0+1.1(f)	mA	ROMCS# = V <sub>IL</sub> , RAMCS# = V <sub>IH</sub> , V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>I/O</sub> = Opens
I <sub>DD2</sub>	RAM Operating Supply Current		2.5+1(f)	mA	ROMCS# = V <sub>IH</sub> , RAMCS# = V <sub>IL</sub> , I <sub>I/O</sub> = Opens
I <sub>SB</sub>	Standby V <sub>DD</sub> Current		10	μA	ROMCS# ≥ V <sub>DD</sub> -0.2V, RAMCS# ≥ V <sub>DD</sub> -0.2V V <sub>IN</sub> ≥ V <sub>DD</sub> -0.2V or V <sub>IN</sub> ≤ 0.2V
V <sub>OL</sub>	Output Low Voltage		0.4	V	I <sub>OL</sub> = 1.0 mA
V <sub>OH</sub>	Output High Voltage	2.2		V	I <sub>OH</sub> = -0.5 mA

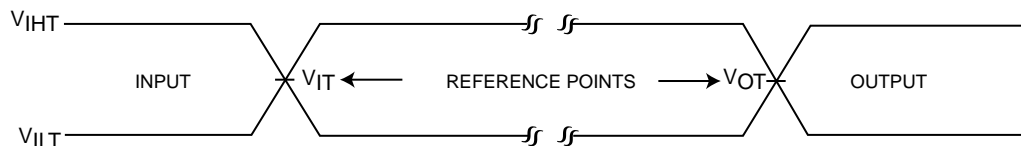
Note: f = 1/cycle time (MHz)

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**TABLE 4: CAPACITANCE (T<sub>a</sub> = 25 °C, f=1 Mhz)**

Parameter	Description	Test Condition	Maximum
C <sub>I/O</sub>	I/O Capacitance	V <sub>I/O</sub> = 0V	8 pF
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6 pF

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AC test inputs are driven at V<sub>IHT</sub> (0.9 V<sub>DD</sub>) for a logic "1" and V<sub>ILT</sub> (0.1 V<sub>DD</sub>) for a logic "0". Measurement reference points for inputs and outputs are V<sub>IT</sub> (0.5 V<sub>DD</sub>) and V<sub>OT</sub> (0.5 V<sub>DD</sub>). Inputs rise and fall times (10% ↔ 90%) are <5 ns.

Note: V<sub>IHT</sub>-V<sub>HIGH</sub> Test  
V<sub>ILT</sub>-V<sub>LOW</sub> Test  
V<sub>IHT</sub>-V<sub>INPUT HIGH</sub> Test  
V<sub>ILT</sub>-V<sub>INPUT LOW</sub> Test

**FIGURE 2: AC INPUT/OUTPUT REFERENCE WAVEFORMS**

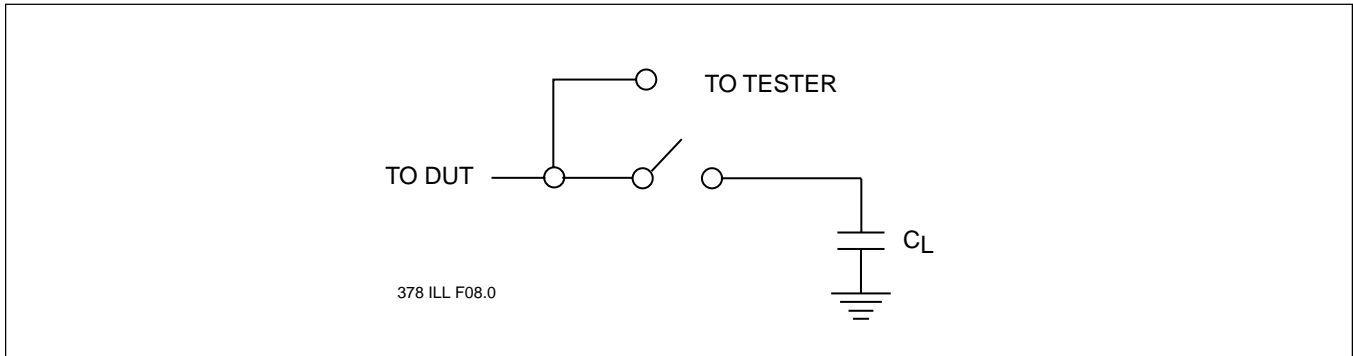


FIGURE 3: A TEST LOAD EXAMPLE

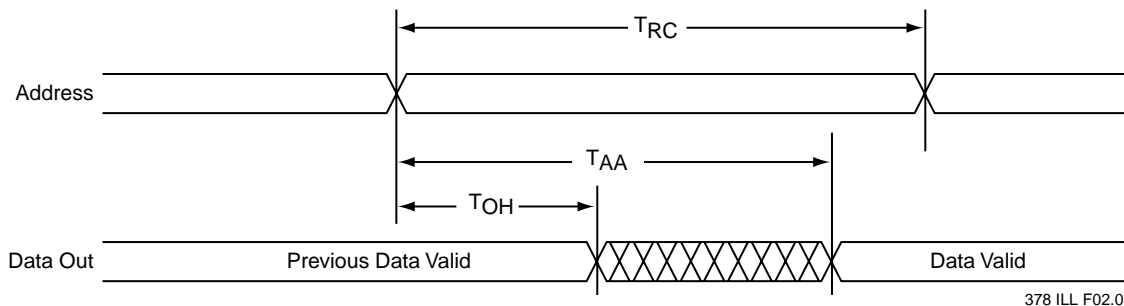
**AC CHARACTERISTICS**

**I. ROM Operation**

TABLE 5: READ CYCLE TIMING PARAMETERS

Symbol	Parameter	V <sub>DD</sub> =3.0 V ± 0.3		Unit
		Min	Max	
T <sub>RC</sub>	Read Cycle Time	500		ns
T <sub>AA</sub>	Address Access Time		500	ns
T <sub>CO</sub>	Chip Select to Output		500	ns
T <sub>OE</sub>	Output Enable to Valid Output		250	ns
T <sub>LZ</sub>	Chip Select to Low-Z Output	10		ns
T <sub>OLZ</sub>	Output Enable to Low-Z Output	10		ns
T <sub>HZ</sub>	Chip Disable to High-Z Output		40	ns
T <sub>OHZ</sub>	Output Disable to High-Z Output		40	ns
T <sub>OH</sub>	Output Hold from Address Change	15		ns

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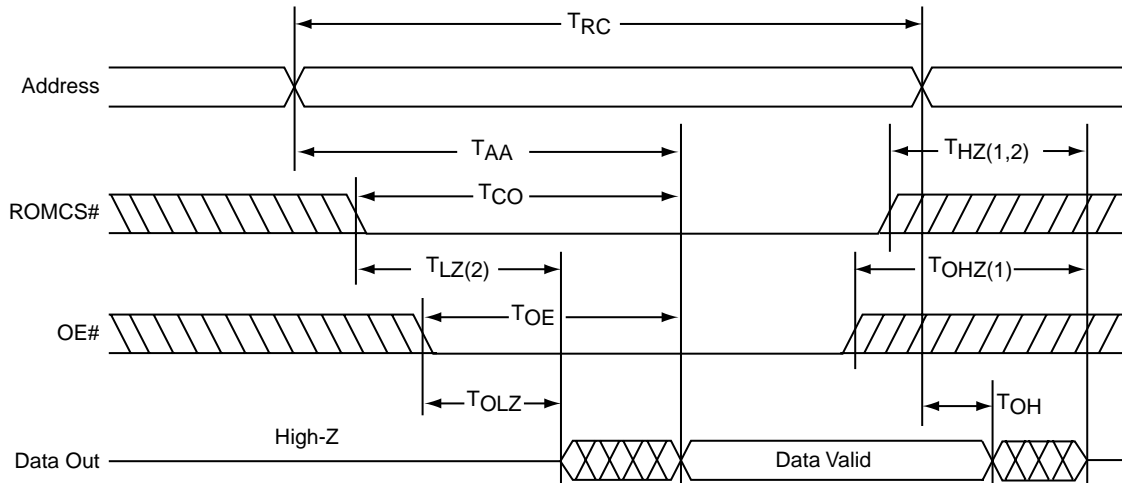
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FIGURE 4: ROM READ CYCLE TIMING DIAGRAM (ADDRESS CONTROLLED) (ROMCS# = OE# = V<sub>IL</sub>)



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- Notes:
1.  $T_{HZ}$  and  $T_{OHZ}$  are defined as the time at which the outputs achieve the open circuit condition and are referenced to the  $V_{OH}$  or  $V_{OL}$ .
  2. At any given temperature and voltage condition  $T_{HZ}(\max)$  is less than  $T_{LZ}(\min)$  both for a given device and from device to device.

**FIGURE 5: ROM READ CYCLE TIMING DIAGRAM (ROMCS# & OE# CONTROLLED)**

## II. SRAM Operation (ROMCS# = $V_{IH}$ )

**TABLE 6: READ CYCLE TIMING PARAMETERS**

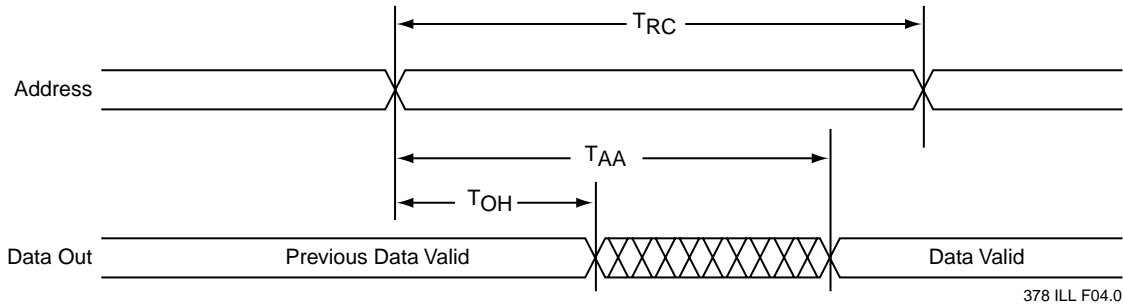
Symbol	Parameter	$V_{DD}=3.0\text{ V} \pm 0.3$		Unit
		Min	Max	
$T_{RC}$	Read Cycle Time	500		ns
$T_{AA}$	Address Access Time		500	ns
$T_{CO}$	Chip Select to Output		500	ns
$T_{LZ}$	Chip Select to Low-Z Output	10		ns
$T_{HZ}$	Chip Disable to High-Z Output		40	ns
$T_{OH}$	Output Hold from Address Change	15		ns

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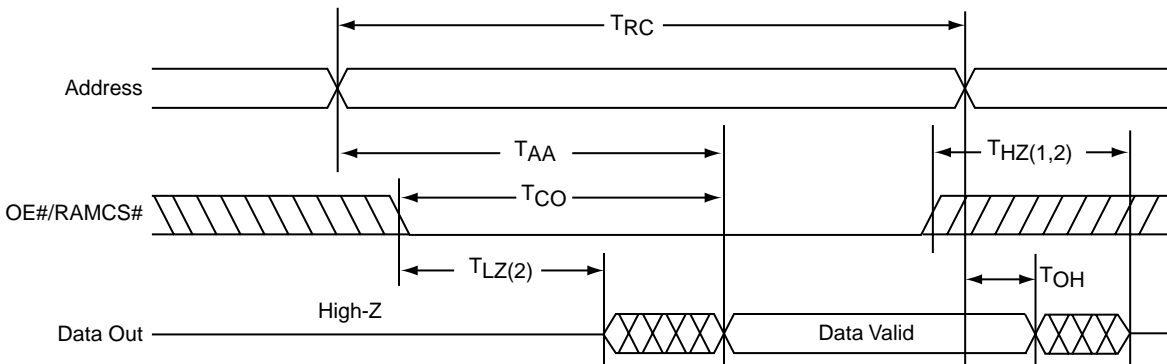
**TABLE 7: WRITE CYCLE TIMING PARAMETERS**

Symbol	Parameter	$V_{DD}=3.0\text{ V} \pm 0.3$		Unit
		Min	Max	
$T_{WC}$	Write Cycle Time	500		ns
$T_{CW}$	Chip Select to End-of-Write	365		ns
$T_{AW}$	Address Valid to End-of-Write	400		ns
$T_{AS}$	Address Set-up Time	0		ns
$T_{WP}$	Write Pulse Width	400		ns
$T_{WR}$	Write Recovery Time	0		ns
$T_{WHZ}$	Write to Output High-Z		80	ns
$T_{DW}$	Data to Write Time Overlap	200		ns
$T_{DH}$	Data Hold from Write Time	0		ns
$T_{OW}$	End Write to Output Low-Z	10		ns

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**FIGURE 6: SRAM READ CYCLE TIMING DIAGRAM (ADDRESS CONTROLLED) ( $OE\#/RAMCS\# = V_{IL}$ ,  $WE\# = V_{IH}$ )**



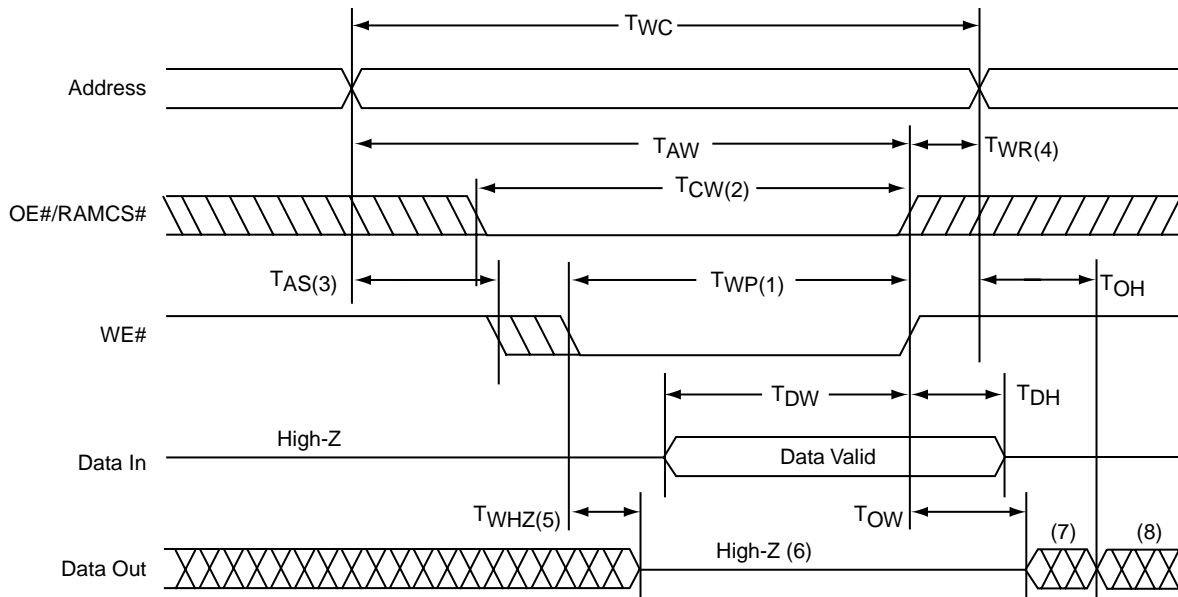
- Notes:
1.  $T_{HZ}$  and  $T_{OHZ}$  are defined as the time at which the outputs achieve the open circuit condition and are referenced to the  $V_{OH}$  or  $V_{OL}$ .
  2. At any given temperature and voltage condition  $T_{HZ}(\max)$  is less than  $T_{LZ}(\min)$  both for a given device and from device to device.
  3.  $WE\#$  is high for Read cycle.

**FIGURE 7: SRAM READ CYCLE TIMING DIAGRAM ( $OE\#/RAMCS\#$  CONTROLLED)**



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- Notes:
1. A write occurs during the overlap ( $T_{WP}$ ) of a low RAMCS# and low WE#. A write begins at the latest transition among RAMCS# going low and WE# going low: A write end at the earliest transition among RAMCS# going high and WE# going high,  $T_{WP}$  is measured from the beginning of write to the end of write.
  2.  $T_{CW}$  is measured from the later of RAMCS# going low to the end of write.
  3.  $T_{AS}$  is measured from the address valid to the beginning of write.
  4.  $T_{WR}$  is measured from the end of write to the address change.
  5. If RAMCS#, WE# are in the read mode during this period, the I/O pins are in the outputs Low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
  6. If RAMCS# goes low simultaneously with WE# going low or after WE# going low, the outputs remain high impedance state.
  7.  $D_{OUT}$  is the same phase of the latest written data in this write cycle.
  8.  $D_{OUT}$  is the read data of new address
  9.  $ROMCS\# = V_{IH}$

**FIGURE 8: SRAM WRITE CYCLE TIMING DIAGRAM**



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TABLE 8: FUNCTIONAL DESCRIPTION/TRUTH TABLE

A0=A18	ROMCS#	OE#/RAMCS# (PIN 32)	WE#	DQ0-DQ7	
X	H	H	X	Z	Standby
A0-A18	L	OE# (H)	X	Z	Output Floating
A0-A18	L	OE# (L)	X	Dout	ROM Read
Only A0-A14 are valid *	H	RAMCS# (L)	H	Dout	RAM Read
Only A0-A14 are valid *	H	RAMCS# (L)	L	Din	RAM Write

\* A15-A18 must be fixed to "L" or "H"

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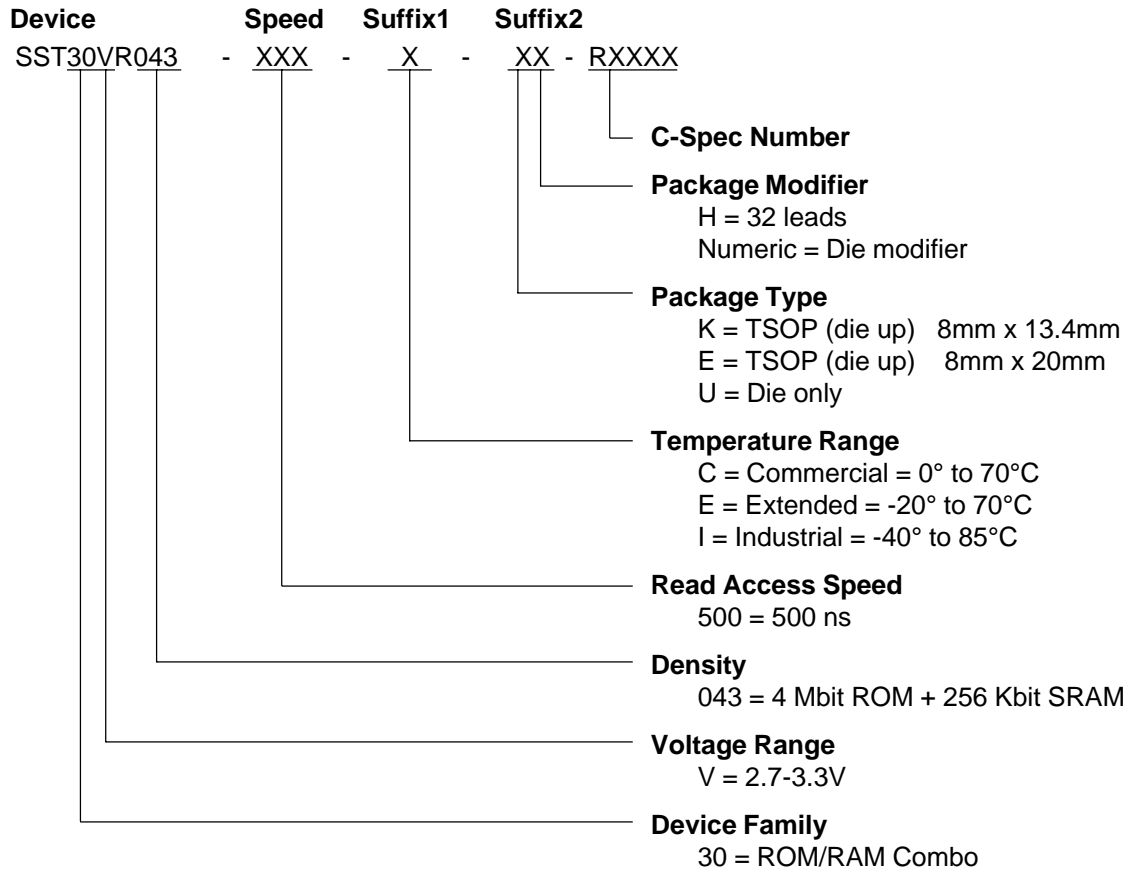
Note: (1) OE# & RAMCS# are pin-shared  
(2) X means Don't Care.



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## SST30VR043

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### SST30VR043 Valid combinations

SST30VR043-500-C-KH	SST30VR043-500-C-EH	SST30VR043-500-C-U1
SST30VR043-500-E-KH	SST30VR043-500-E-EH	
SST30VR043-500-I-KH	SST30VR043-500-I-EH	

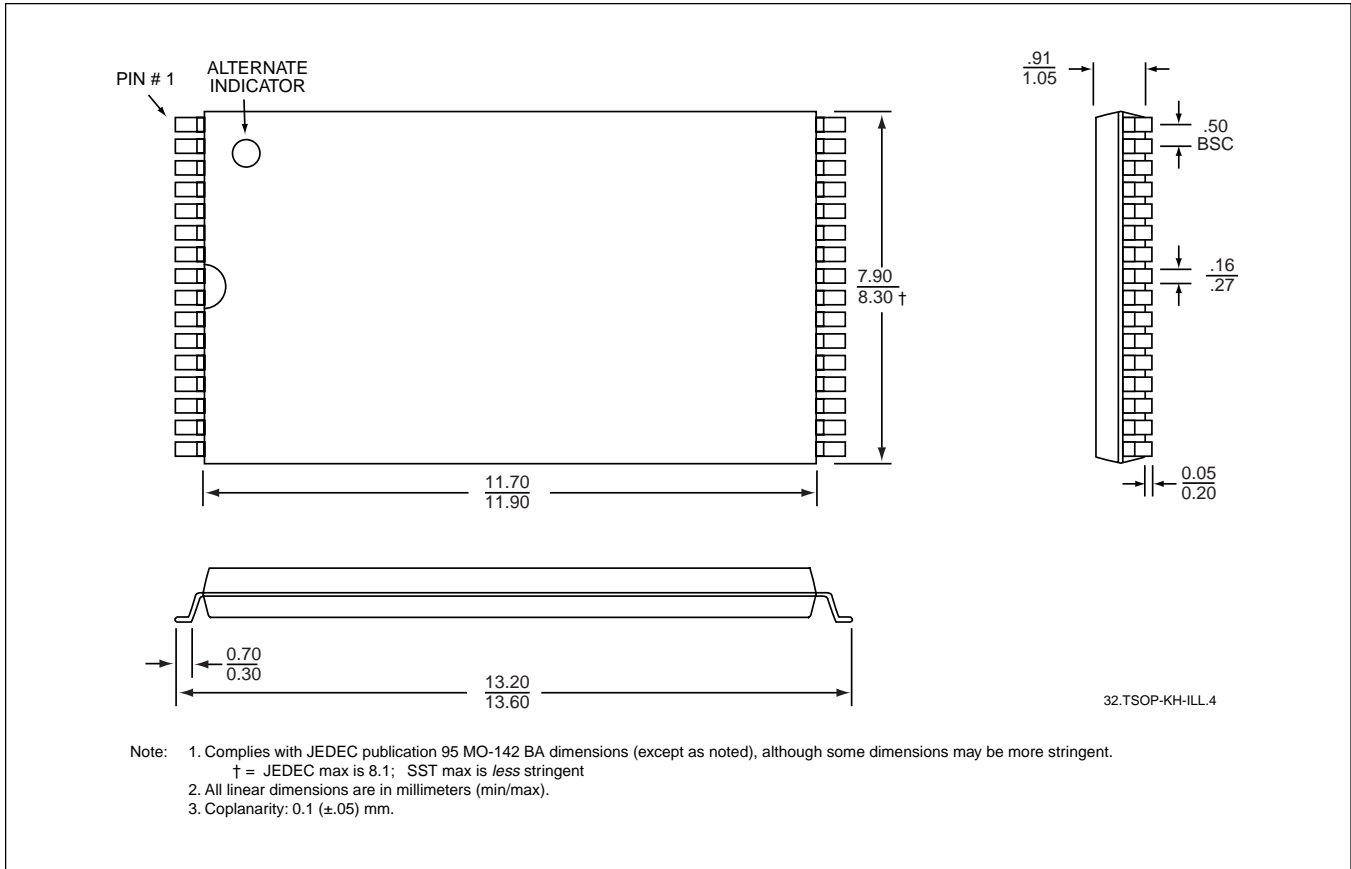
**Example:** Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.



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## PACKAGING DIAGRAMS

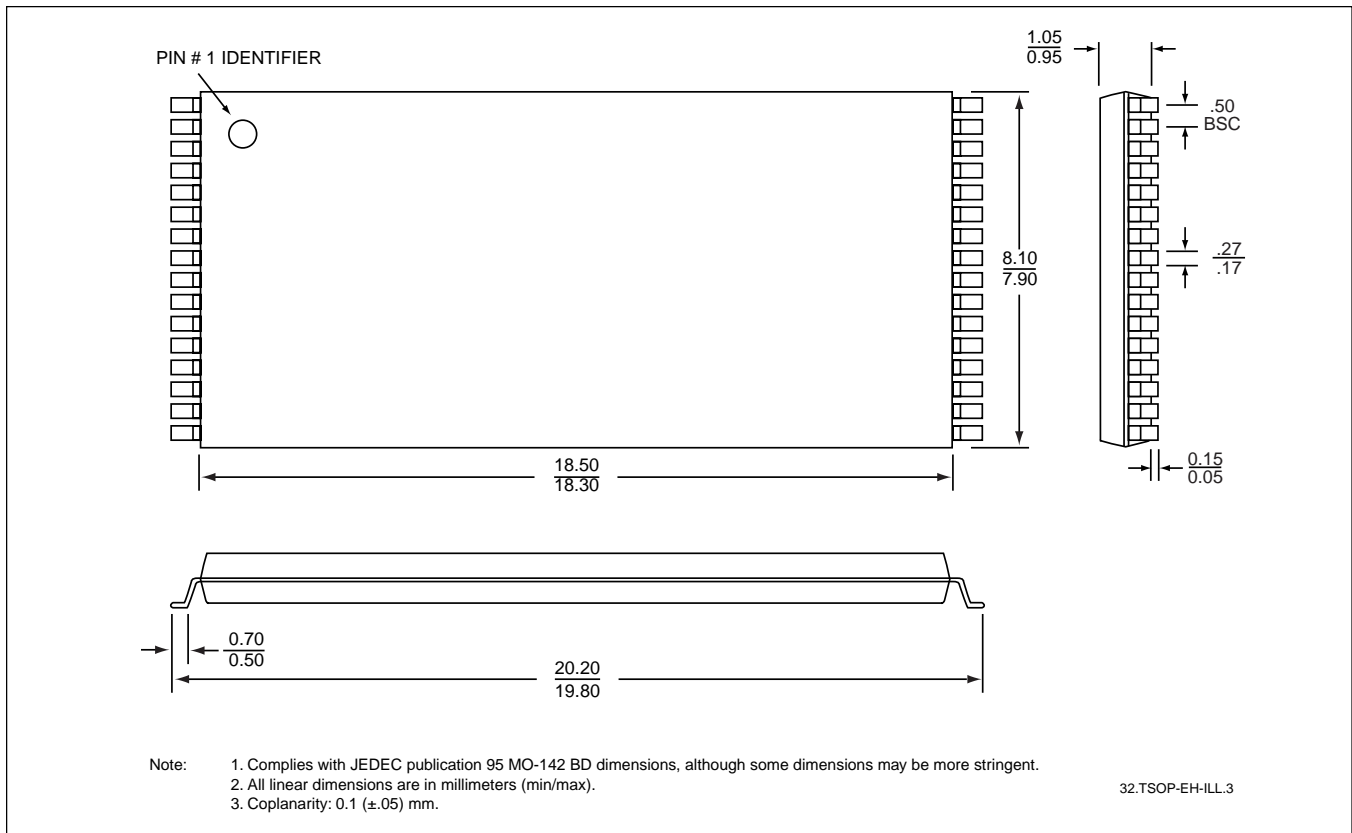


**32-PIN THIN SMALL OUTLINE PACKAGE (TSOP) 8MM X 13.4MM**  
**SST PACKAGE CODE: KH**



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**32-PIN THIN SMALL OUTLINE PACKAGE (TSOP) 8MM X 20MM**  
**SST PACKAGE CODE: EH**



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