

Design Considerations for the SST FlashFlex51 Family Microcontroller



Application Note
August 1999

1.0 INTRODUCTION

The following design considerations outline applications of generally accepted PCB design practices to prevent data corruption issues that could be encountered when using single power-supply microcontrollers with embedded EEPROM such as the SST89F54/58 devices.

The types of data corruption encountered are described below:

- False Write occurs during an intentional write cycle, when either the data loaded or address loaded is incorrect.
- Inadvertent Write occurs when a valid write command is issued unintentionally.

The causes of these problems are described below:

- A noisy circuit can cause False Writes as well as Inadvertent Writes. These errors can be minimized using generally accepted board layout and decoupling practices.
- Incorrect power-up / power-down sequence can cause Inadvertent Writes. Correct power-up and power-down sequences can minimize these errors.
- An inadequate power-on ramp rate can cause Inadvertent Writes. Considering the ramp rate when tuning the external power-on reset circuit can minimize these errors.

The following sections discuss the application considerations to address these specific issues.

2.0 GENERAL BOARD LAYOUT GUIDELINES

Reliable operation in a high-frequency analog and digital environment requires that some basic board layout rules be followed. SST recommends implementing generally accepted PCB design practices in order to minimize noise. They include:

- The preferred method of designing a high-speed application is on a printed circuit board, where the user can control the layout of power and ground planes. Many high-speed applications that are laid out on a wire wrap board will not work reliably.
- Use a PC board with separate GND and V_{DD} planes. Ensure that the connection between each supply pin and the corresponding power/ground plane is as short as possible (less than 6 mm).

- Use wide traces for V_{DD} . For the SST89F54/58 devices with maximum I_{DD} of 45 mA, use a minimum trace width of 4 mils.
- Trace widths for GND should be twice that of V_{DD} .
- Keep all bypass capacitors as close to the power pins of the device as possible. If a socket is used, add an additional 1-10 μF capacitor between V_{DD} and V_{SS} .
- Specifically for the SST89F54/58 devices, use high quality RF grade capacitors. SST recommends a high frequency 0.1 μF ceramic capacitor to be placed as close as possible between V_{DD} and V_{SS} , i.e. less than 1 cm away from the V_{DD} pin of the device. Additionally, a low frequency 4.7 μF electrolytic capacitor from V_{DD} to V_{SS} should be placed within 5 cm of the V_{DD} pin.
- Ensure that the power supply does not have more than 100 mV of peak-to-peak noise at the device's V_{DD} pins. Make this check while sending random data, both during power-on ramp and in steady state operation.

3.0 EXTERNAL POWER-ON RESET CIRCUIT

When powering up any microcontroller, the power supply voltage must traverse the full voltage range (0 to V_{DD}) before the power supply voltage reaches its final operating level. Some circuits on the device (e.g., logic) will start operating at voltage levels lower than other circuits on the chip (e.g., flash memory); therefore, some circuits may power up in an unknown state. Powering up the device without a valid reset could cause the microcontroller to start executing instructions from an indeterminate location. Such undefined states may cause an inadvertent write to the flash.

To guarantee that the SST89F54/58 devices start up in a known state, the system application must contain a power-on reset circuit. When power is applied to the SST89F54/58 devices, the RST pin must be held high long enough for the external oscillator to start up, in addition to the required two machine cycles for a valid power-on Reset. A common method to extend the RST signal is to implement a RC circuit by connecting the RST pin to V_{DD} through a 10 μF capacitor and to V_{SS} through an 8.2 K resistor as shown in Figure 1. Provisions must be made to ensure the V_{DD} rise time, T_R , does not exceed 1 ms. For an external oscillator with slow start-up time, the reset signal must be extended in order to account for the delay. The time taken for the oscillator to start up often varies depending on the manufacturer, e.g.



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the start up times varied from 63 – 113 ms on tests of various manufacturer's 24 MHz frequency crystals.

A system reset initializes the SST89F54/58 devices and begins program execution at program memory location 0000h. The reset input for the SST89F54/58 devices is the RST pin. In order to reset the SST89F54/58 devices, a logic level high must be applied to the RST pin for at least two machine cycles (24 clock cycles), after the external oscillator becomes stable. ALE and PSEN# are internally pulled high during reset. During reset, ALE and PSEN# output a high level in order to perform a correct reset; therefore, the ALE and PSEN# pins must not be driven to 0 while reset is active. Driving ALE and PSEN#

low could cause the device to go into an indeterminate state. The RC circuit described above maintains the maximum delay time allowed between V_{DD} and RST ramp, T_{VR} (10 ns) as shown in Figure 2.

SST recommends a power-up sequence asserting logic level high on RST, ALE and PSEN#, as well as asserting a logic low on EA# prior to the V_{DD} ramp, for the two machine cycles after the oscillator becomes stable, as shown in Figure 3. The recommended power-down sequence is shown in Figure 4. The recommended power-up / power-down sequences will provide maximum protection against the effects of external factors, such as a noisy power supply.

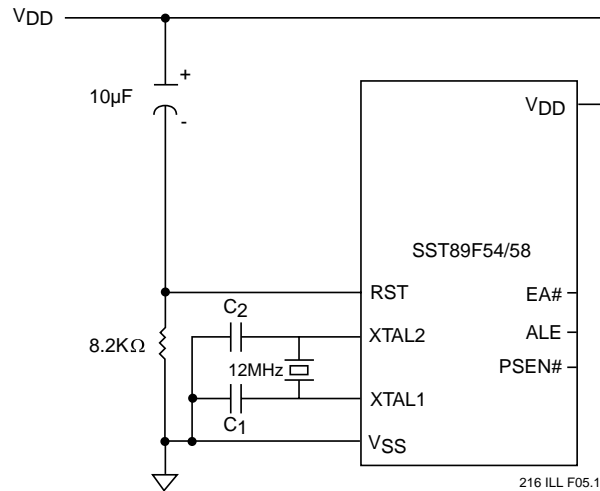


FIGURE 1: RECOMMENDED POWER-ON RESET CIRCUIT

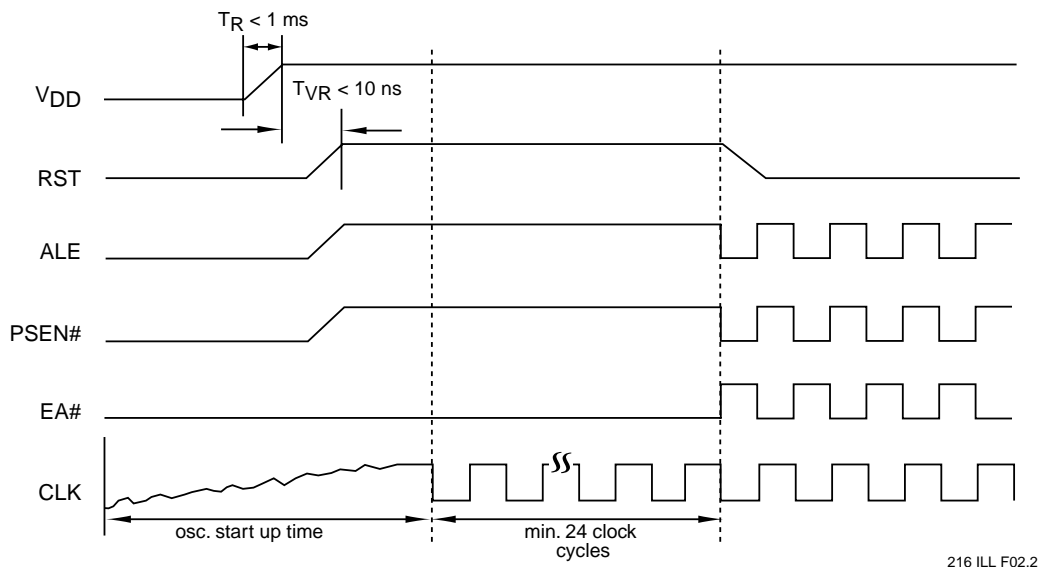


FIGURE 2: POWER-UP SEQUENCE



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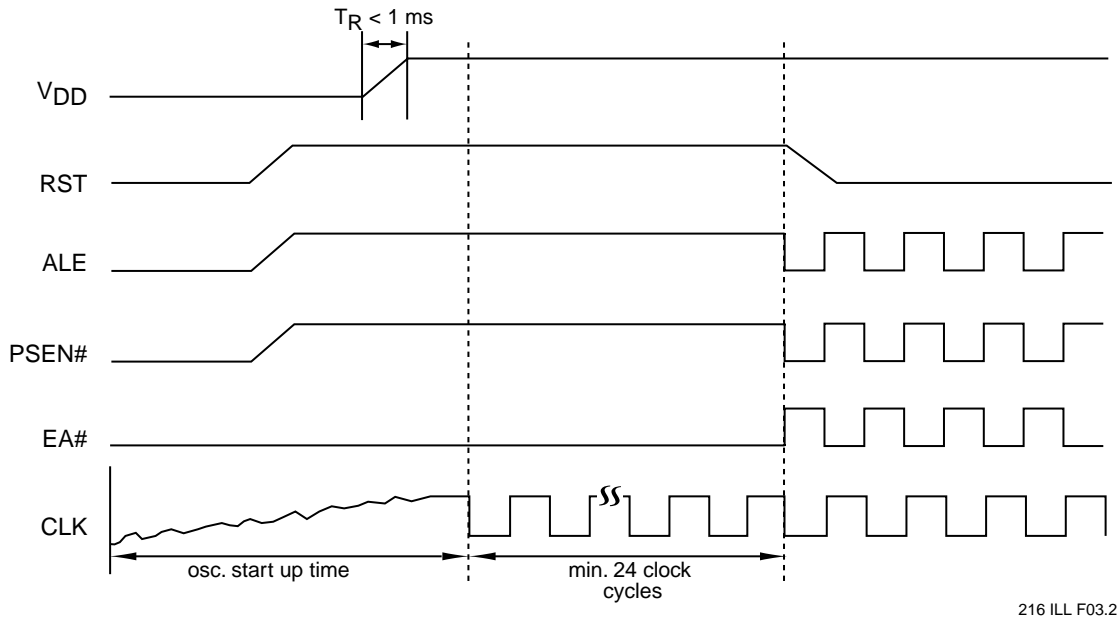


FIGURE 3: RECOMMENDED POWER-UP SEQUENCE

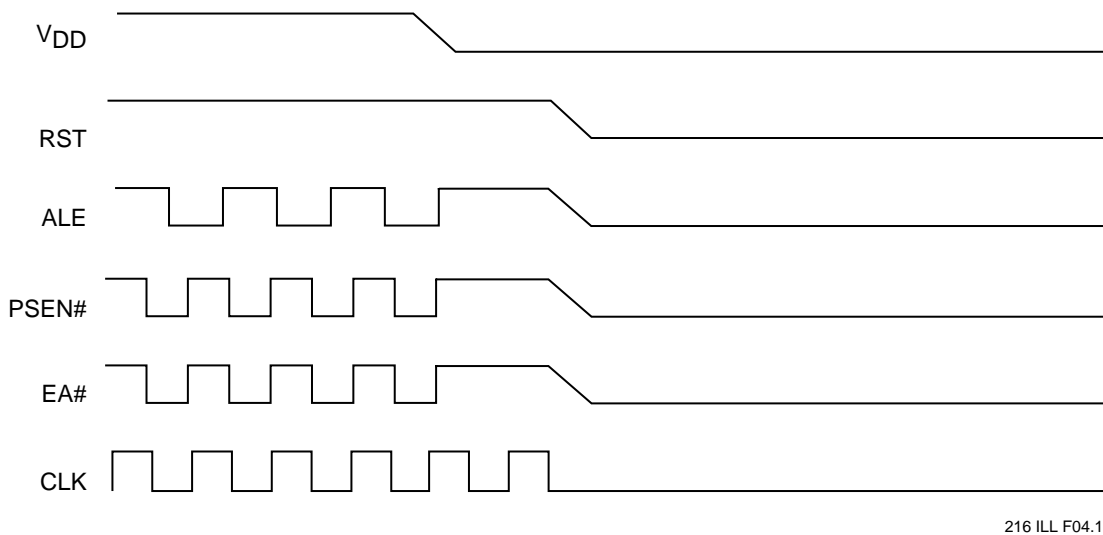


FIGURE 4: RECOMMENDED POWER-DOWN SEQUENCE

3.0 SUMMARY

SST recommends implementing generally accepted PCB design practices and the recommended power-up/power-down sequences when using the SST89F54/58 devices in a design. These recommendations can help

avoid many data corruption issues that could be encountered when using single power-supply microcontrollers with embedded EEPROM.



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